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INTEL(R) PENTIUM(R) M PROCESSOR

INTEL(R) 82855GME GMCH

INTEL(R) 82801DB I/O CONTROLLER HUB 4

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REVISION HISTORY

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NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.

2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.

3. VCC = +5V UNLESS OTHERWISE SPECIFIED.

4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.

5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.

6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

855GME

CRB SCHEMATICS

2-DDR SDRAM, 8 LAYER, ATX

FAB B

REV 1.4

PBA: C24895-202

POWER SYMBOLS USED:

VCC3

VCC

VCCP

+12V

-12V

NOTES:

1. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.

2. VCC = +5 VOLTS UNLESS OTHERWISE SPECIFIED.

3. VCC3 = +3.3 VOLTS UNLESS OTHERWISE SPECIFIED.

4. VCCP = +1.05 VOLTS UNLESS OTHERWISE SPECIFIED.

5. * SUFFIX INDICATES ACTIVE LOW SIGNAL.

6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

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INTEL CORPORATION

5000 W. CHANDLER BLVD

CHANDLER, AZ 85226

DOCUMENT NUMBER

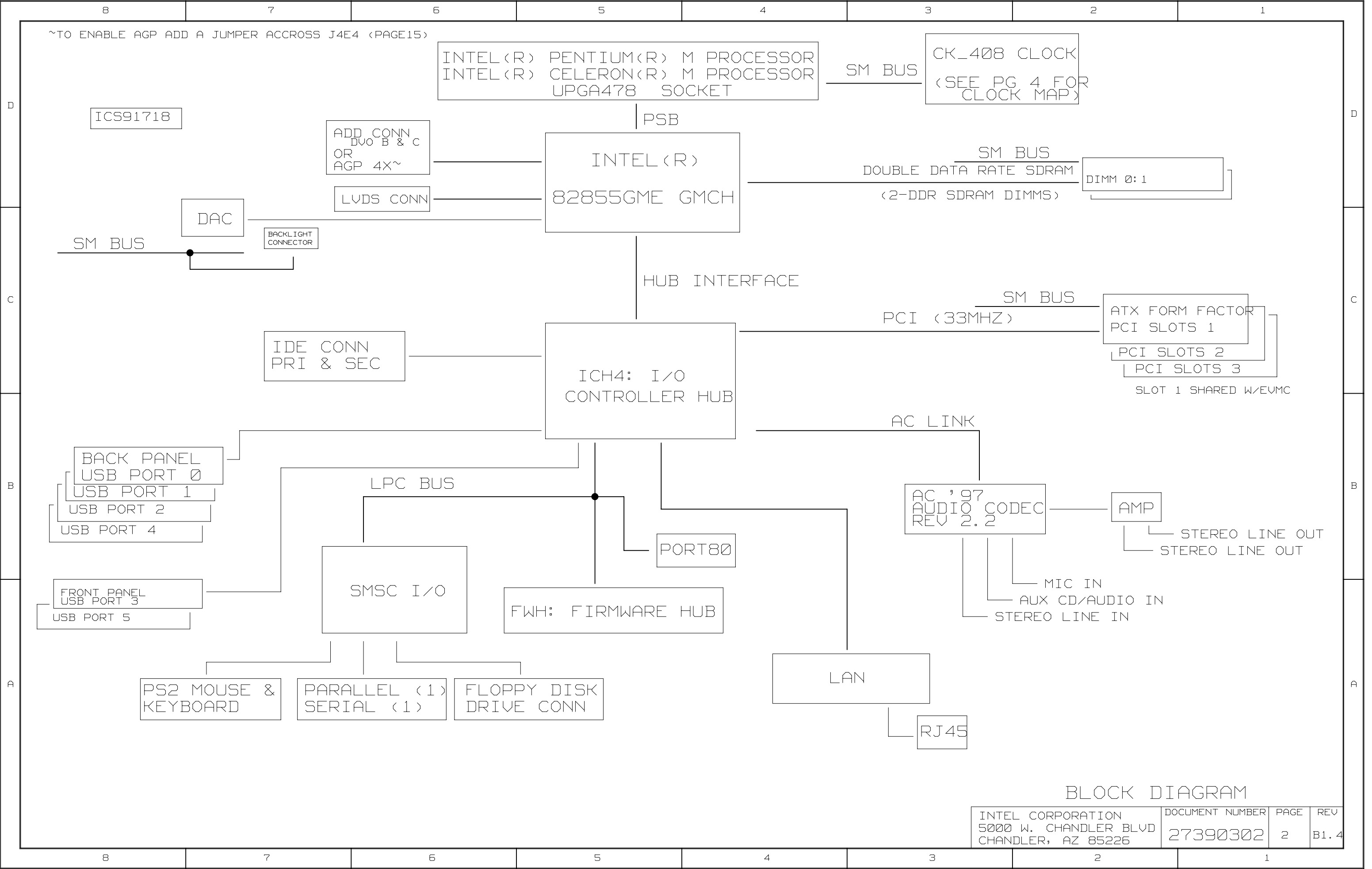
27390302

PAGE

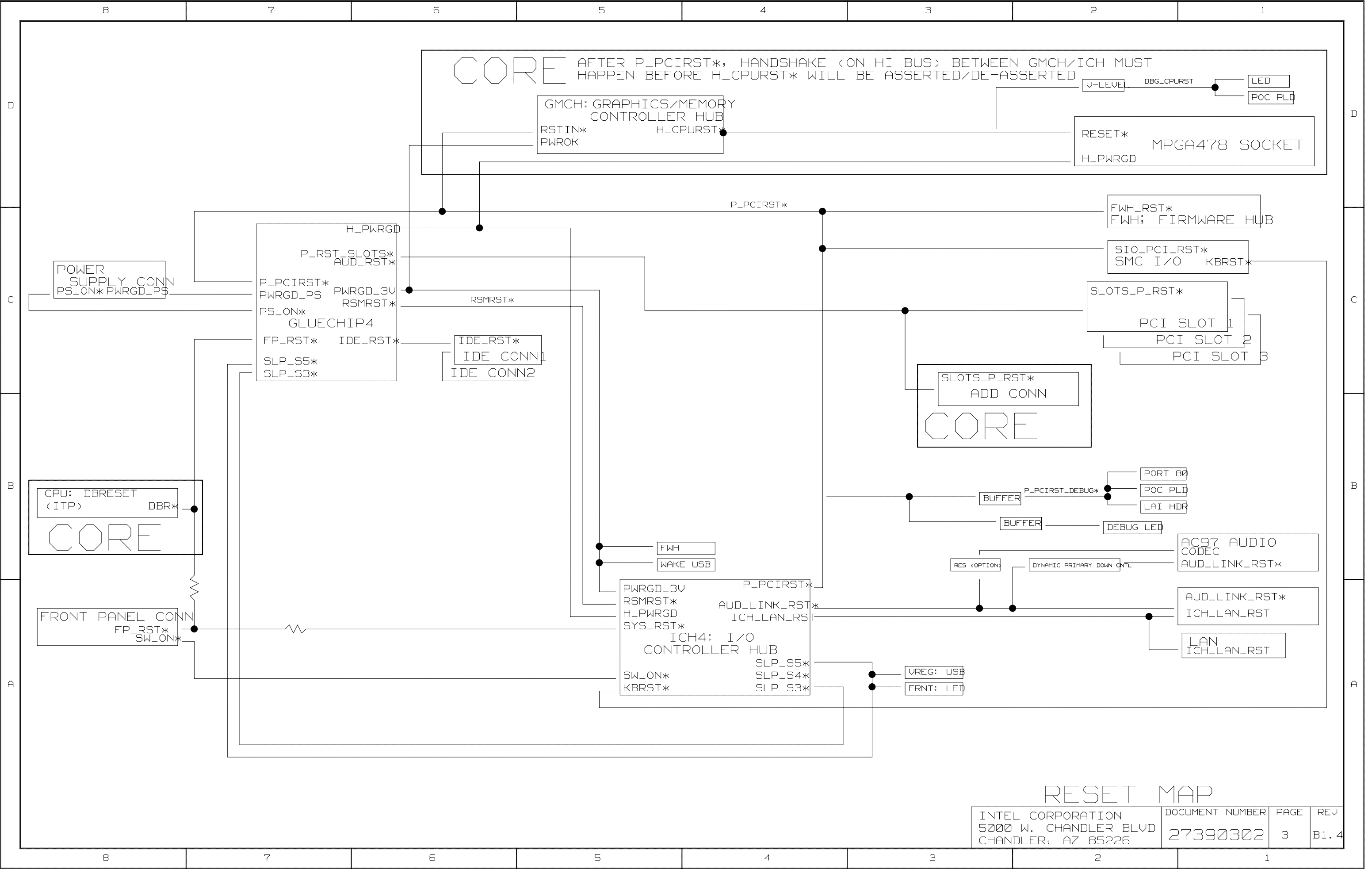
1/75

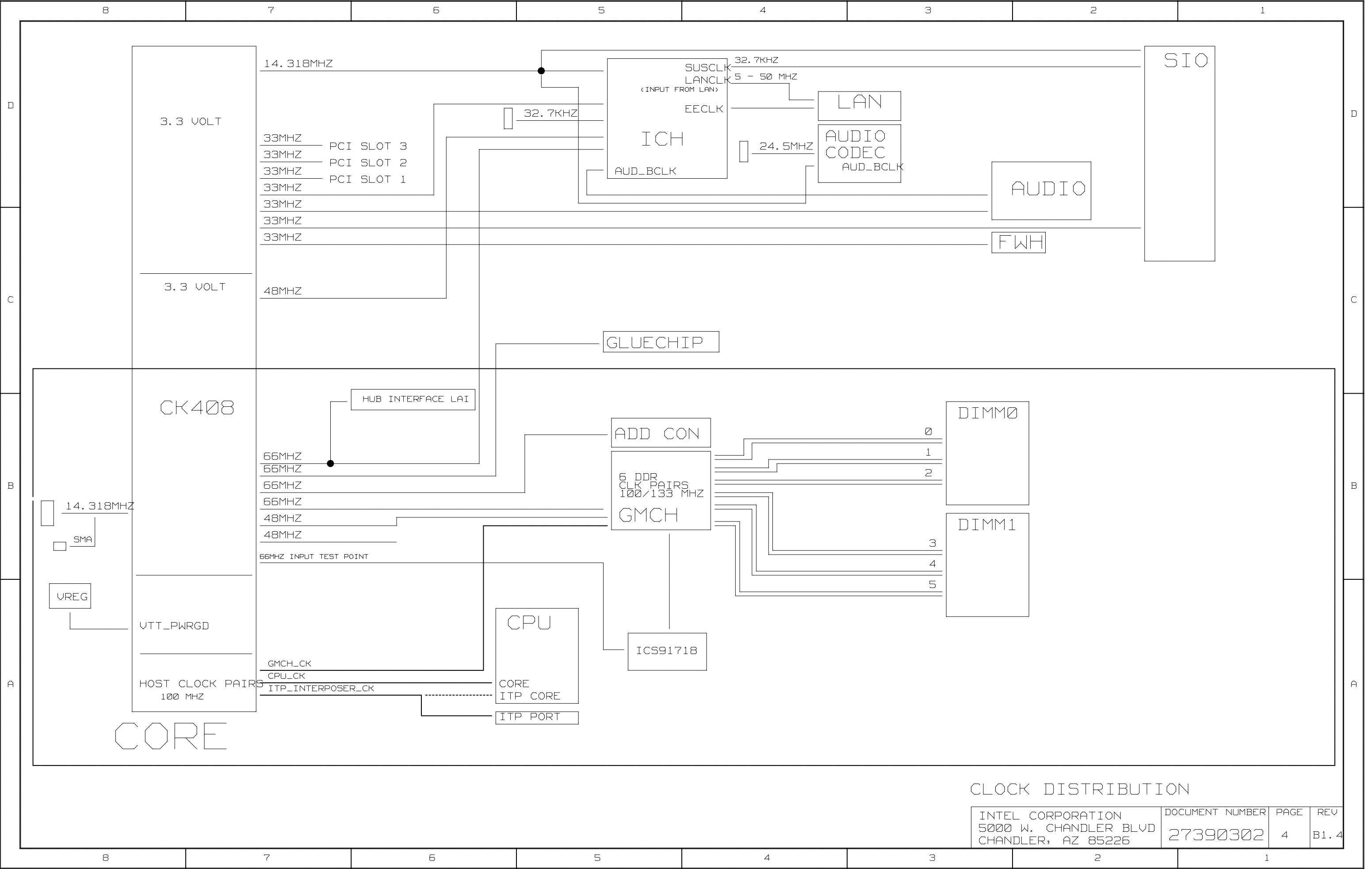
REV

B1.4

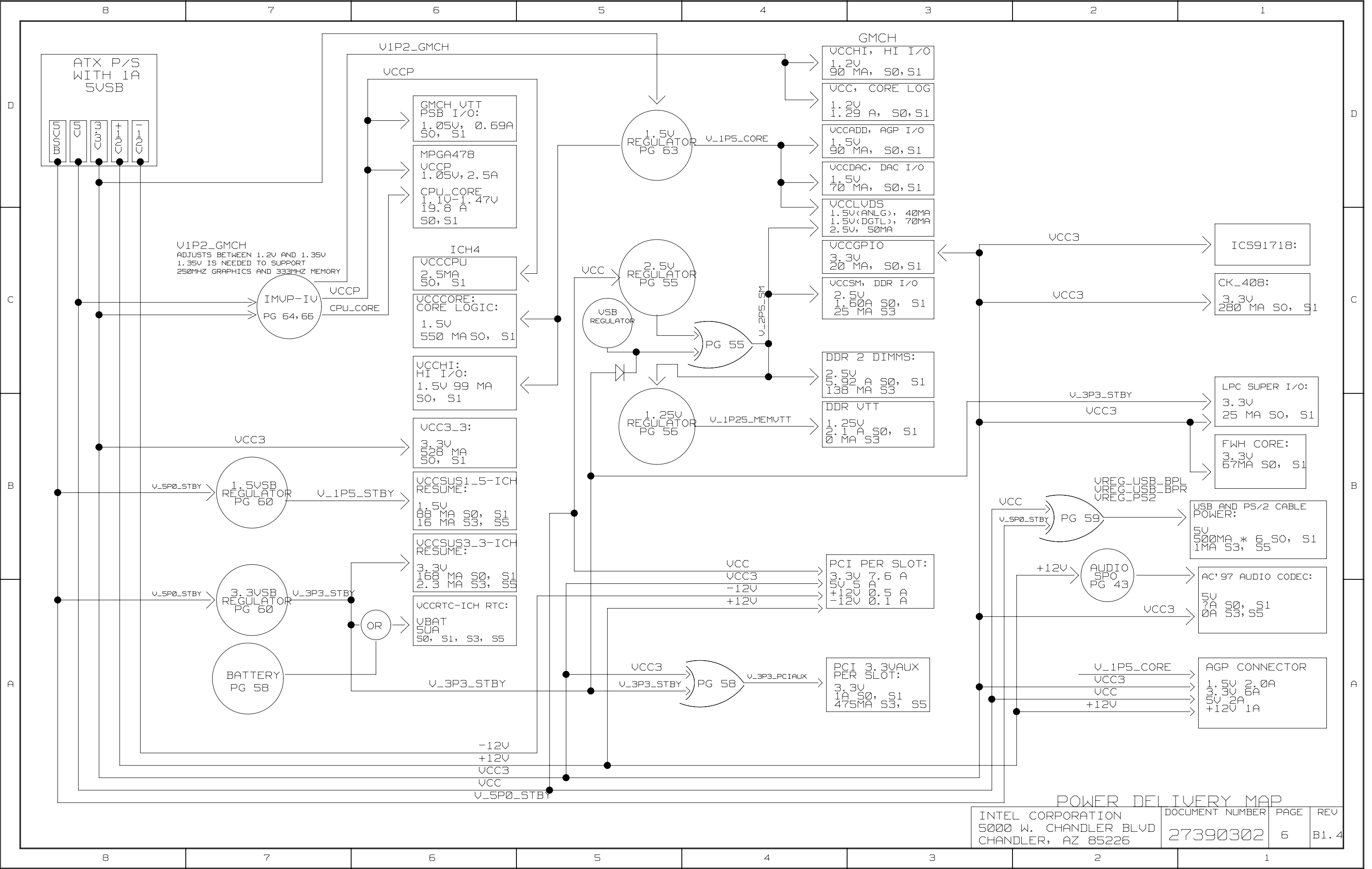


BLOCK DIAGRAM



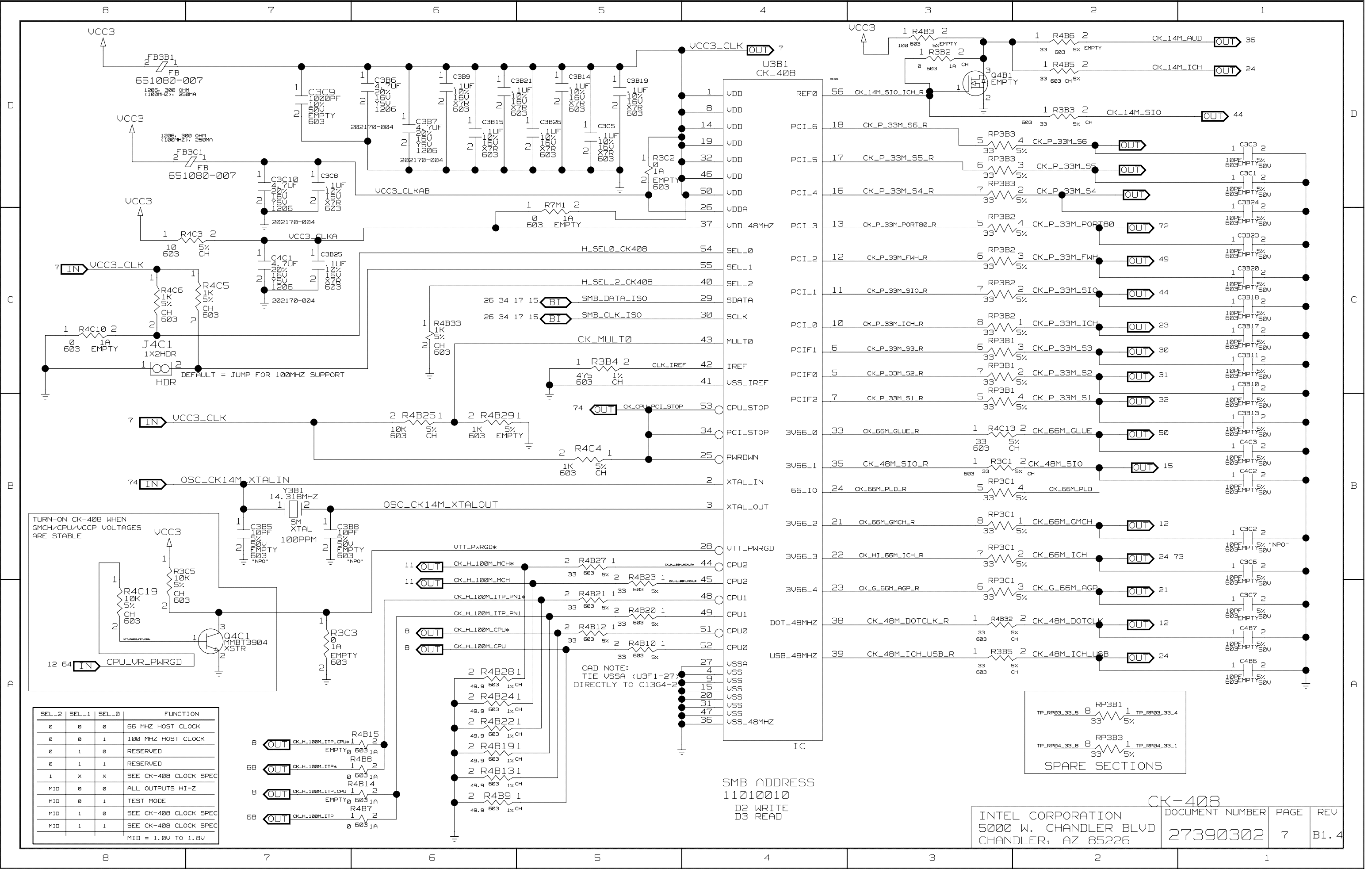


CLOCK DISTRIBUTION



POWER DELIVERY MAP

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 27390302	PAGE 6	REV B1.4
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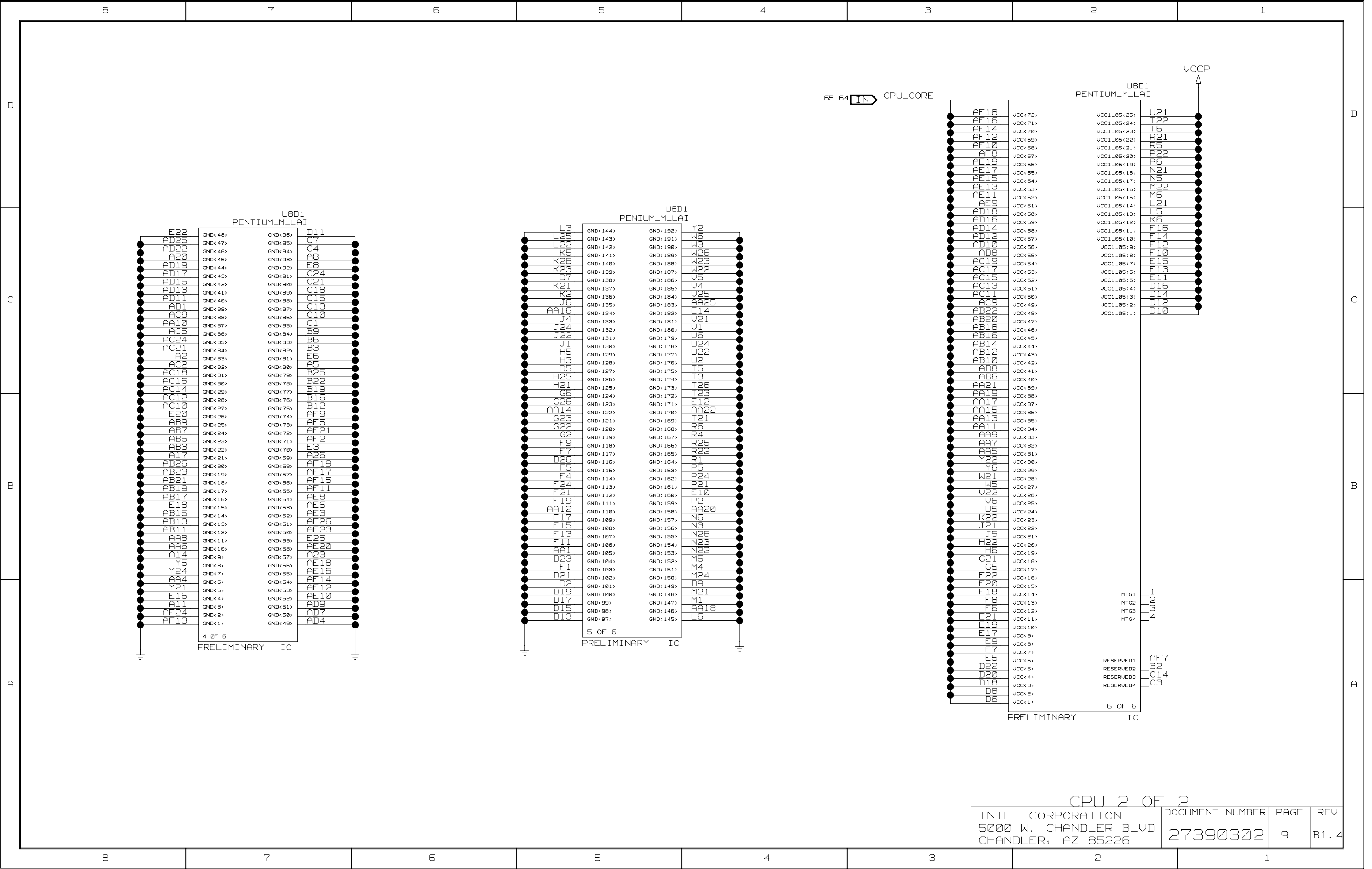


SEL_2	SEL_1	SEL_0	FUNCTION
0	0	0	66 MHz HOST CLOCK
0	0	1	100 MHz HOST CLOCK
0	1	0	RESERVED
0	1	1	RESERVED
1	x	x	SEE CK-408 CLOCK SPEC
MID	0	0	ALL OUTPUTS HI-Z
MID	0	1	TEST MODE
MID	1	0	SEE CK-408 CLOCK SPEC
MID	1	1	SEE CK-408 CLOCK SPEC

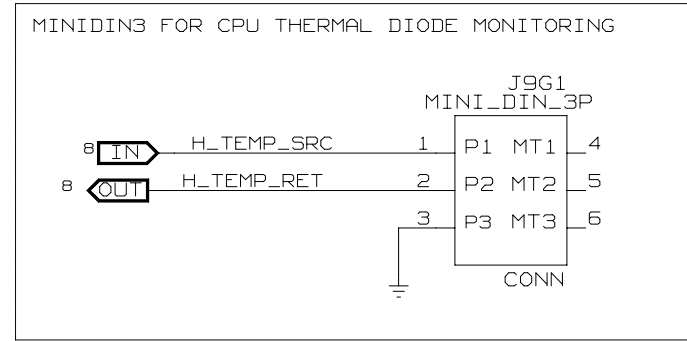
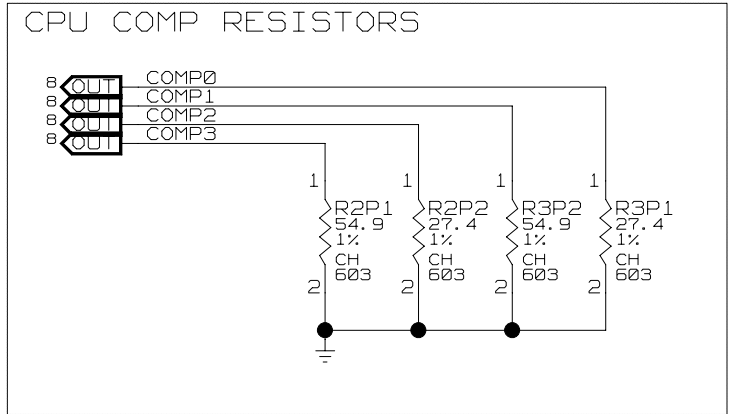
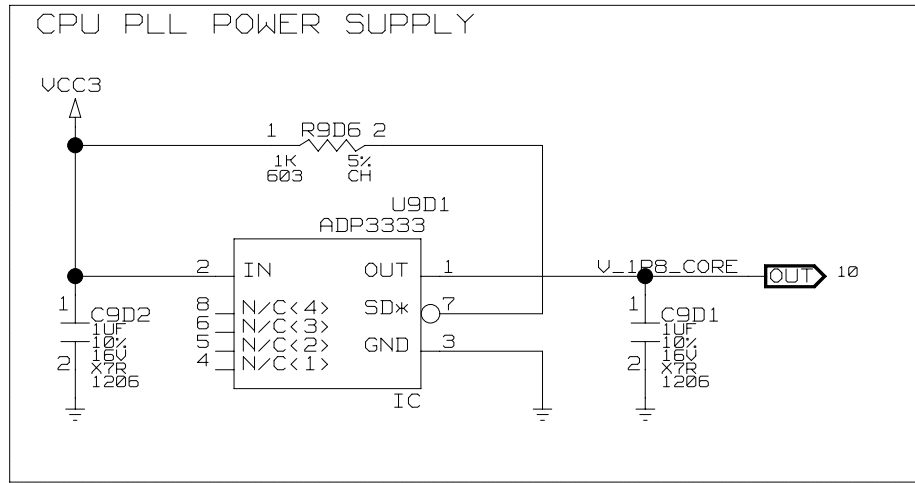
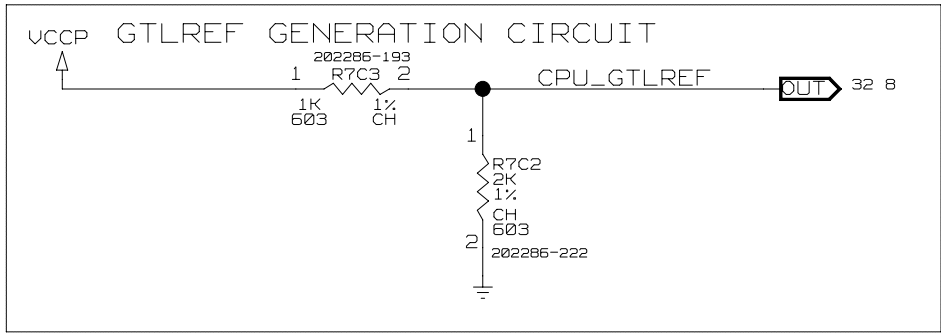
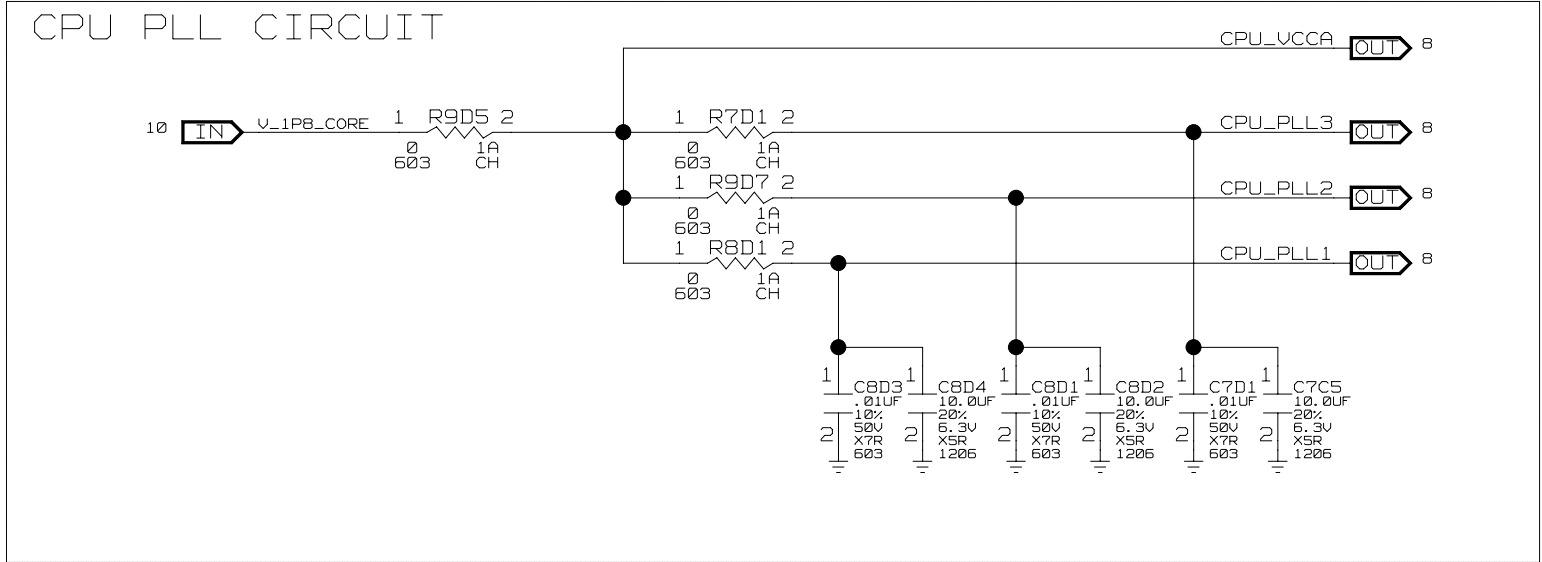
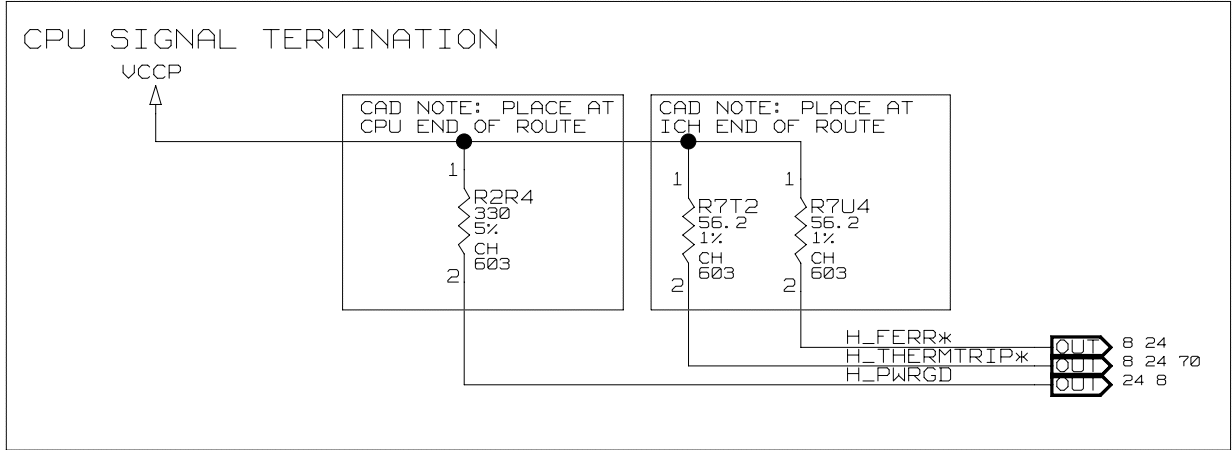
MID = 1.0V TO 1.8V

TP_RP03_33_5	8	RP3B1	1	TP_RP03_33_4
33		5%		
TP_RP04_33_8	8	RP3B3	1	TP_RP04_33_1
33		5%		

SPARE SECTIONS

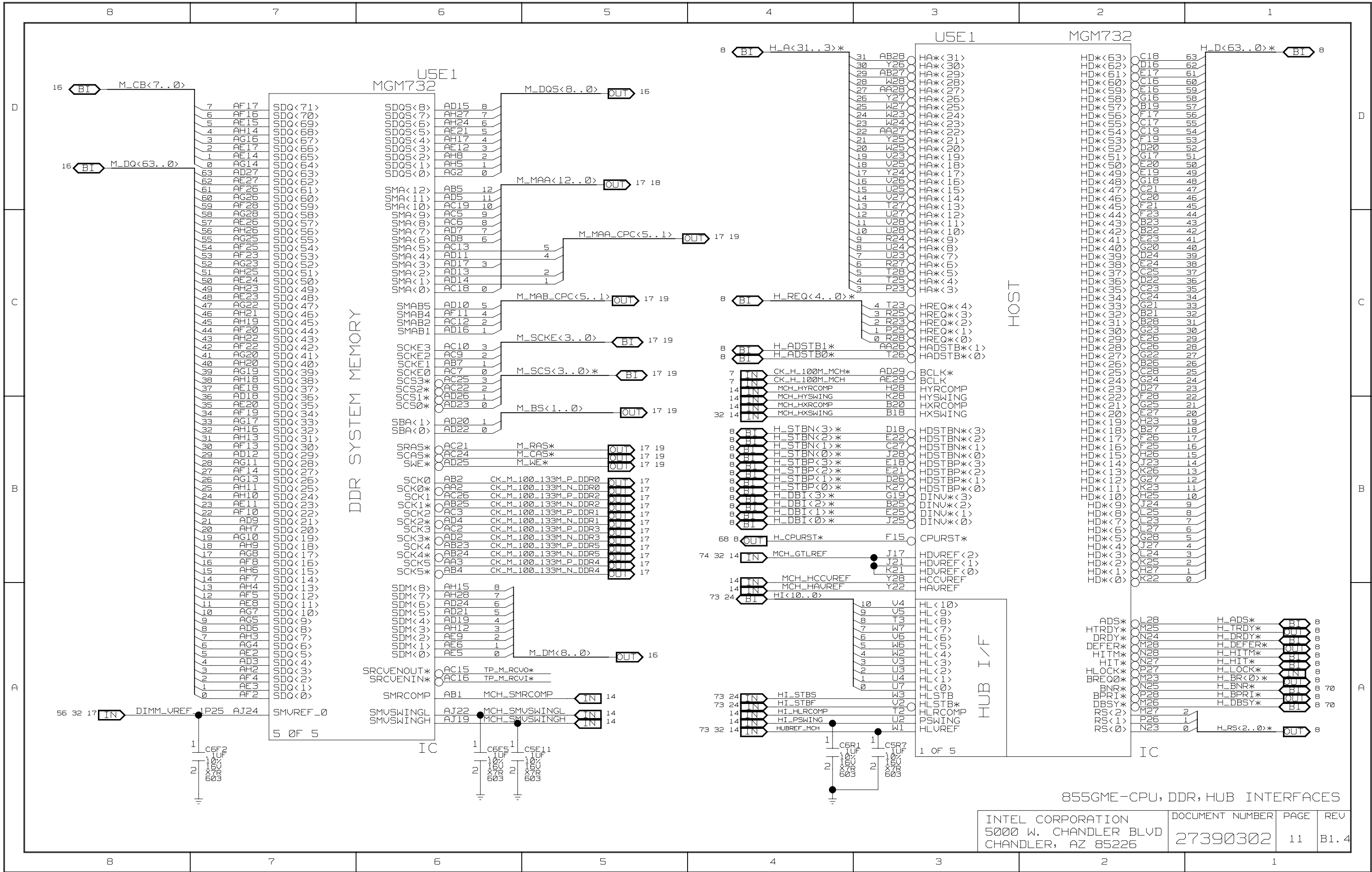


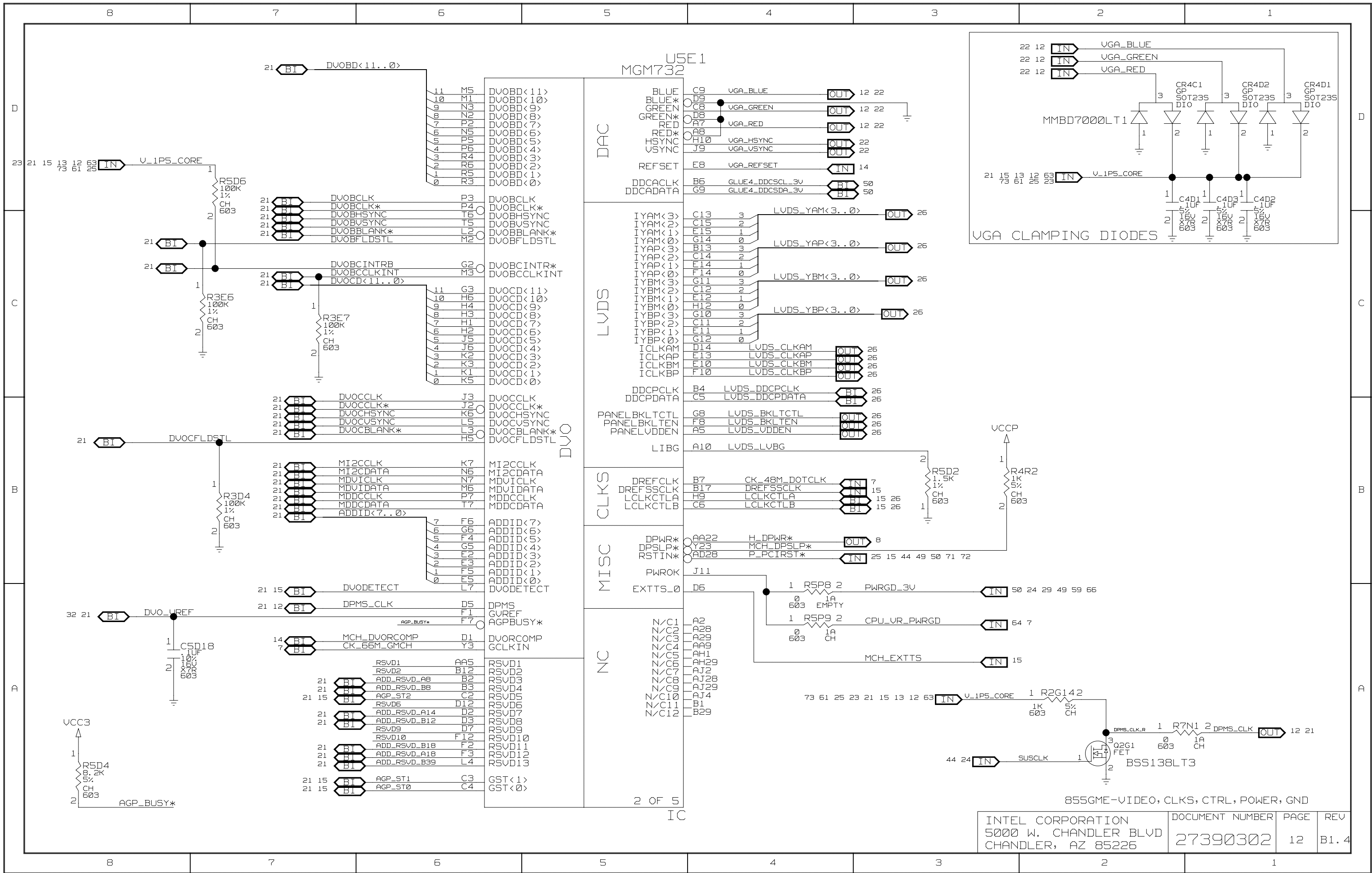
CPU 2 OF 2

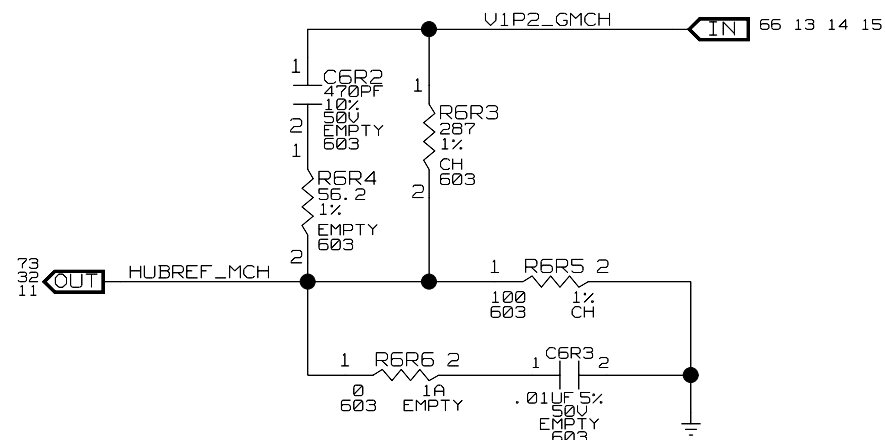
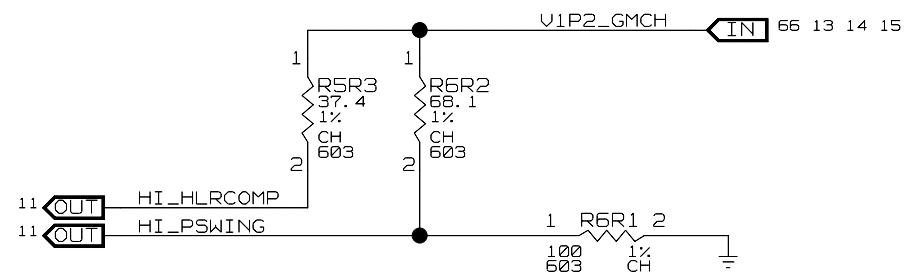


CPU CIRCUITS

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 27390302	PAGE 10	REV B1.4
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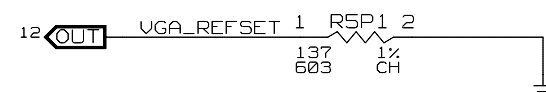


GMCH CORE VOLTAGE TABLE

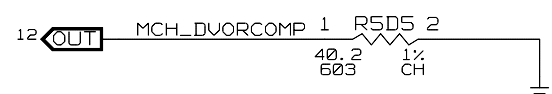
RESISTOR	1.2V	1.35V
R6R3	243, 1%	287, 1%
R5R3	27.4, 1%	37.4, 1%
R6R2	49.9, 1%	68.1, 1%

NOTE: SEE PG66 FOR RELATED STUFFING OPTIONS

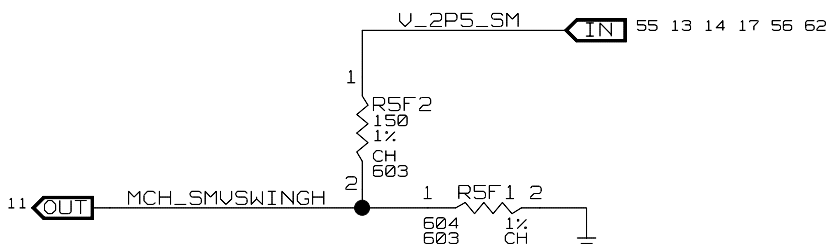
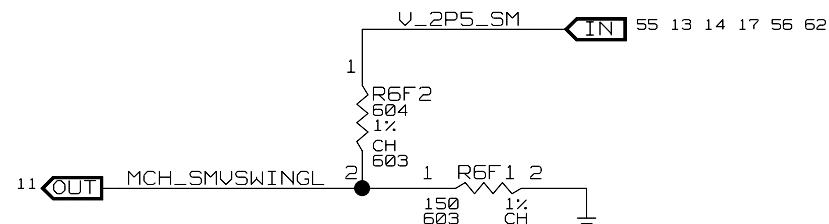
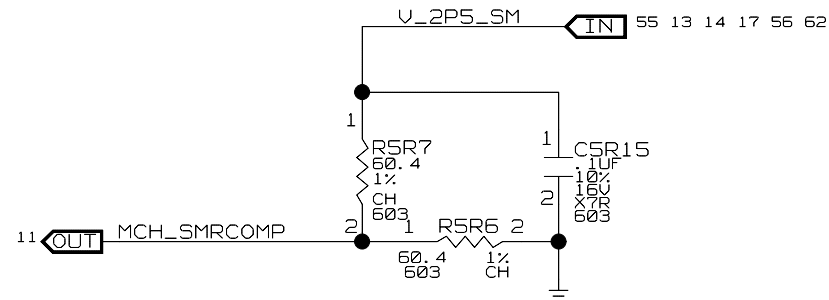
DAC



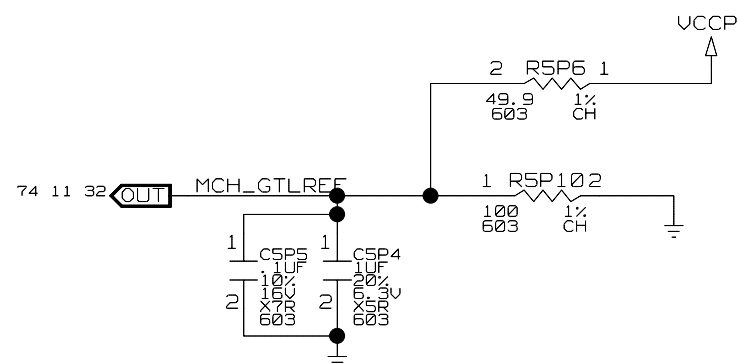
DVO



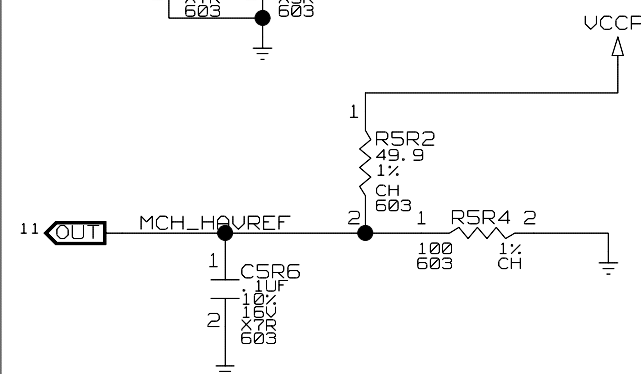
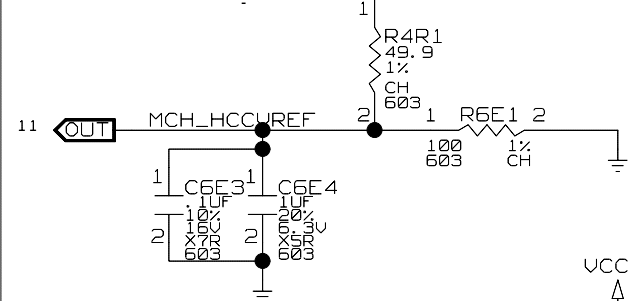
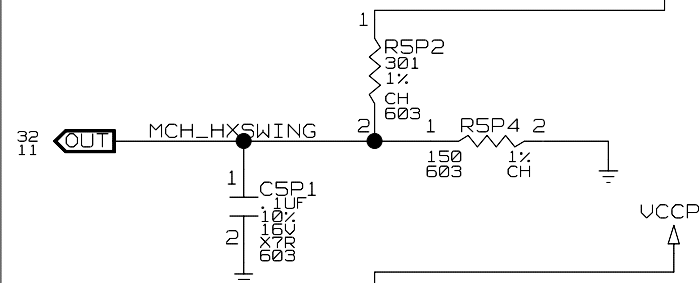
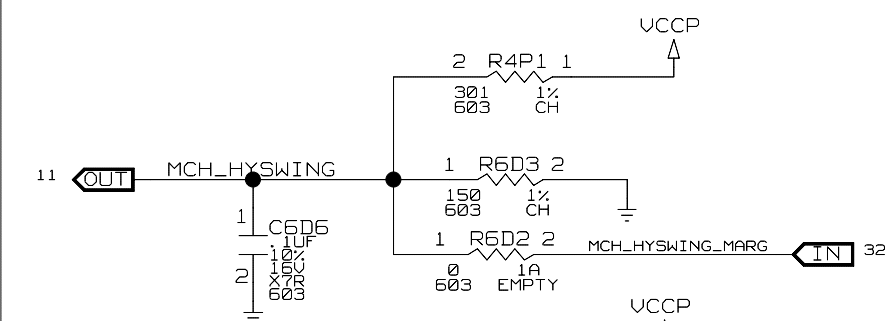
MEMORY



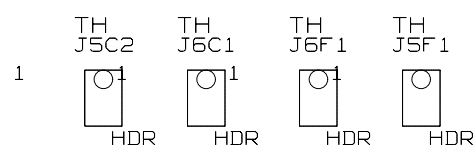
GTL



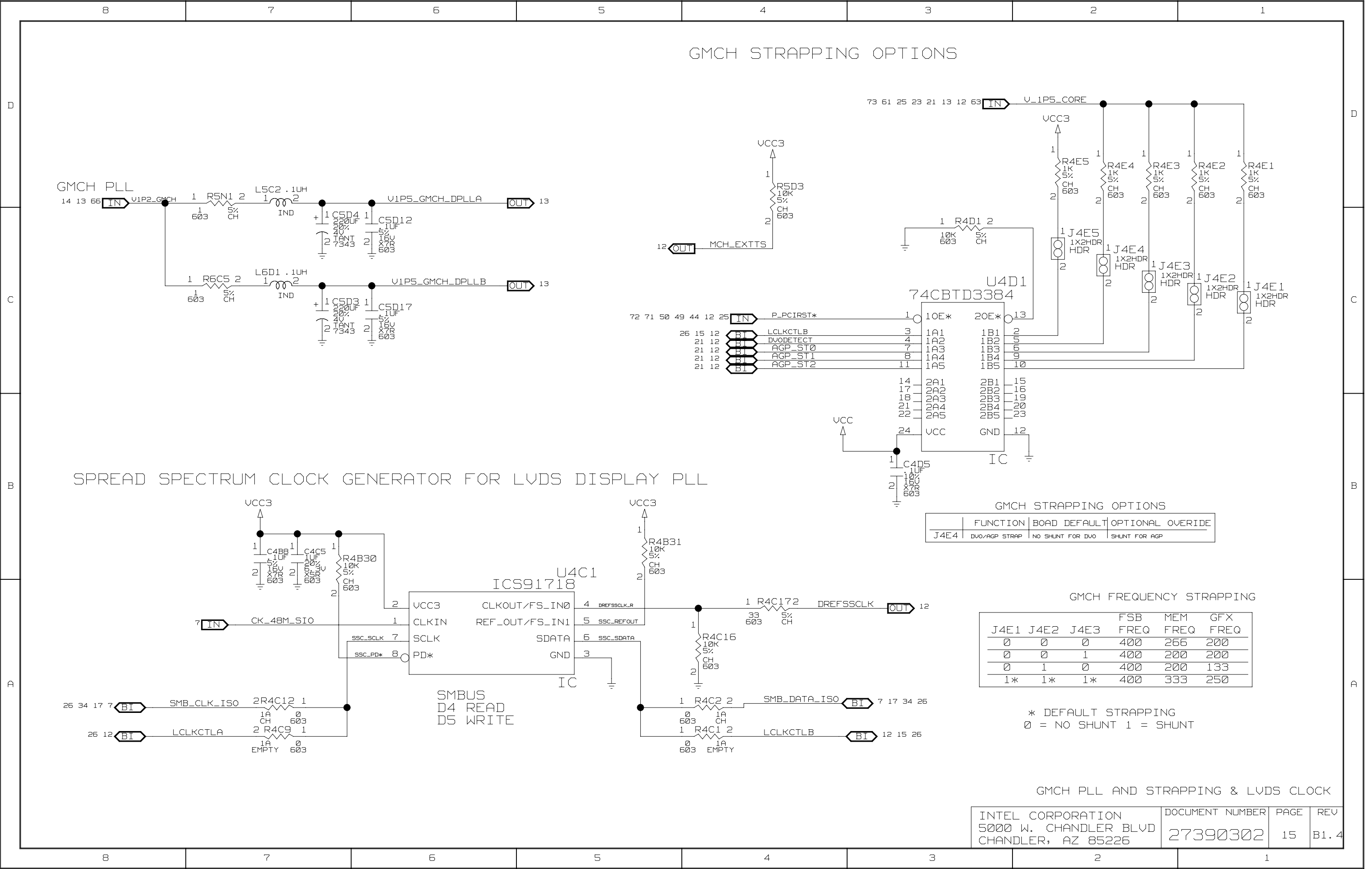
MCH COMPENSATION & REFERENCE VOLTAGE

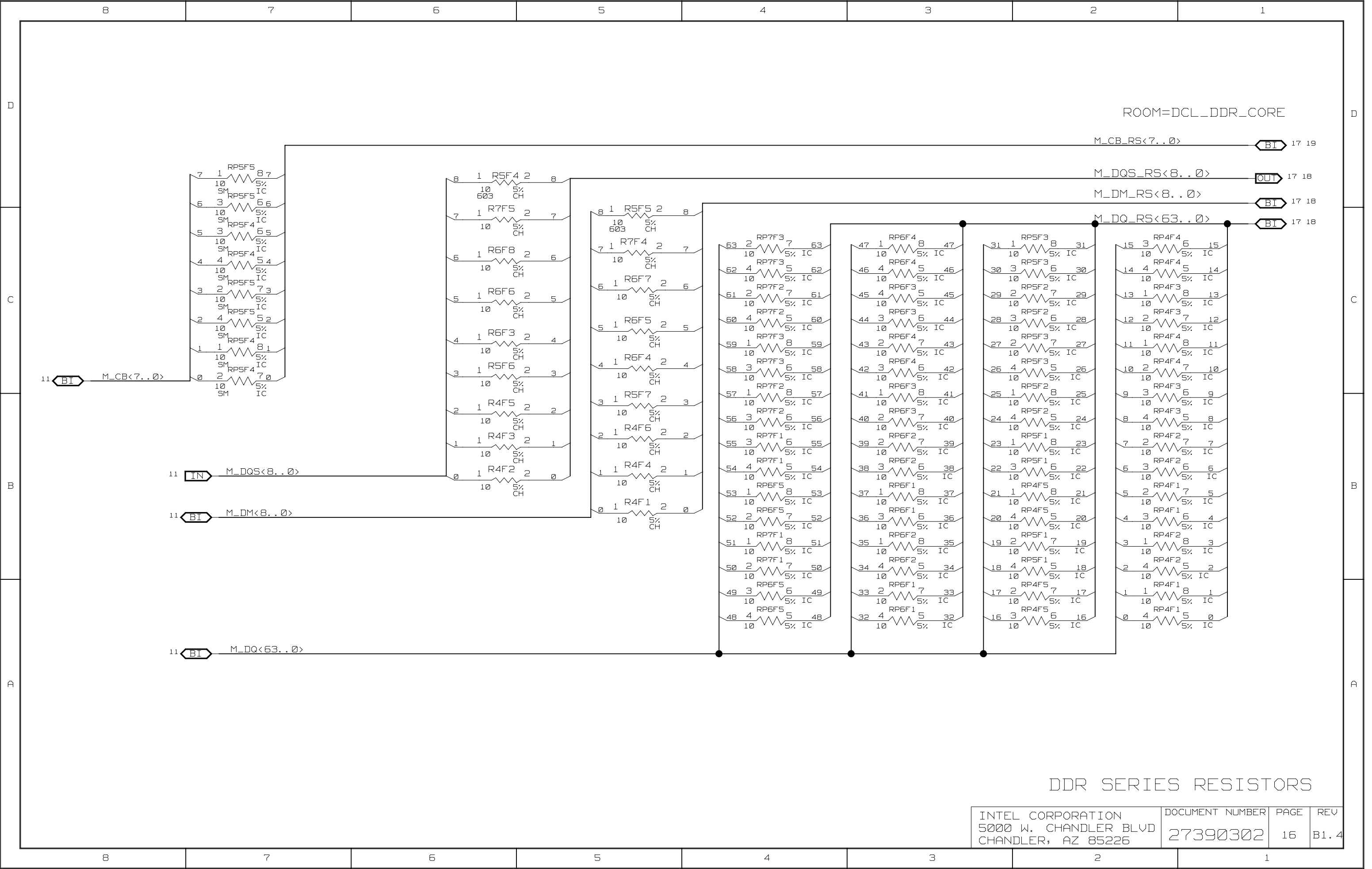


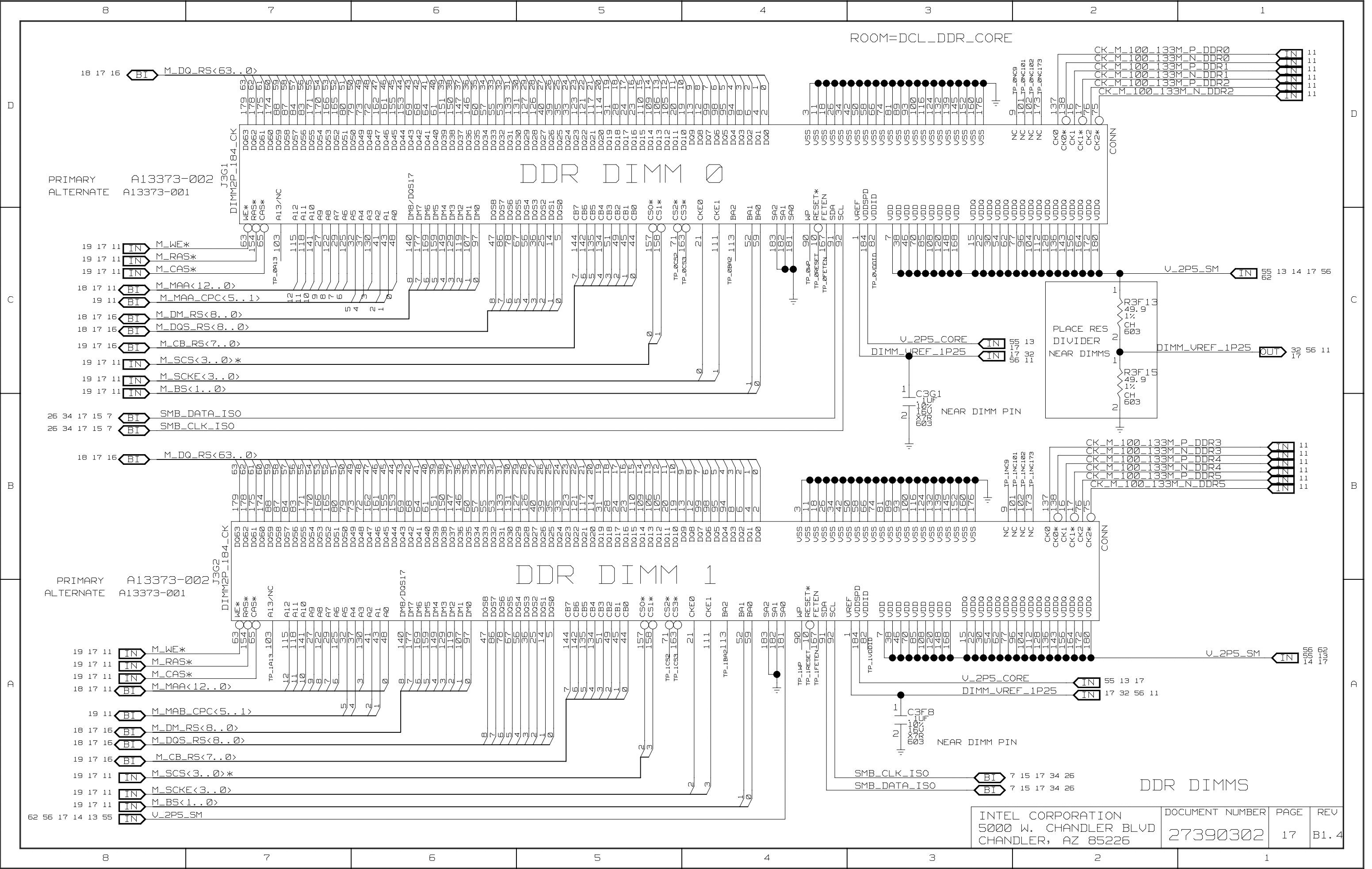
HEATSINK RETENTION CLIPS: QTY(4)

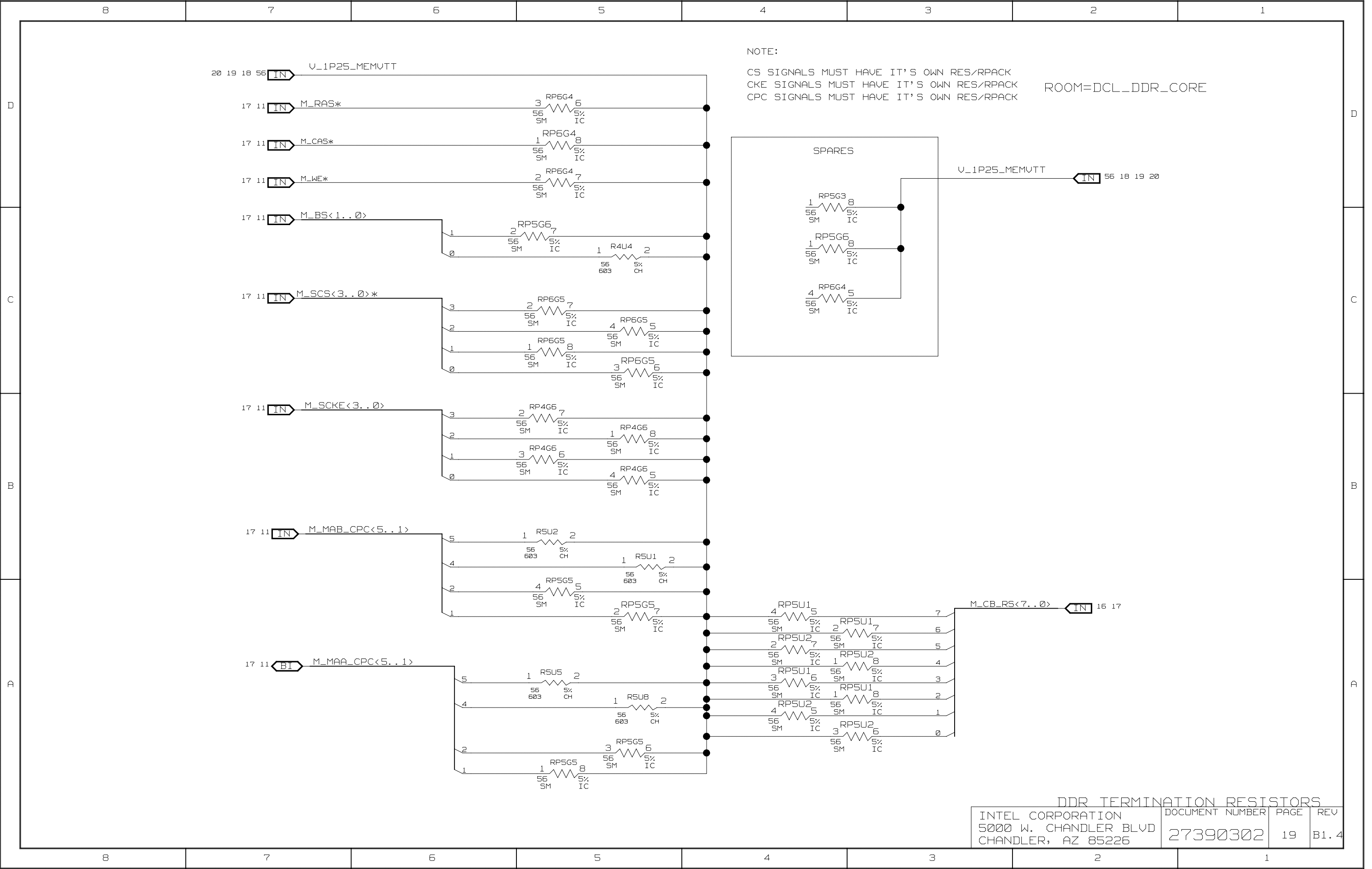


855GME-CIRCUITRY



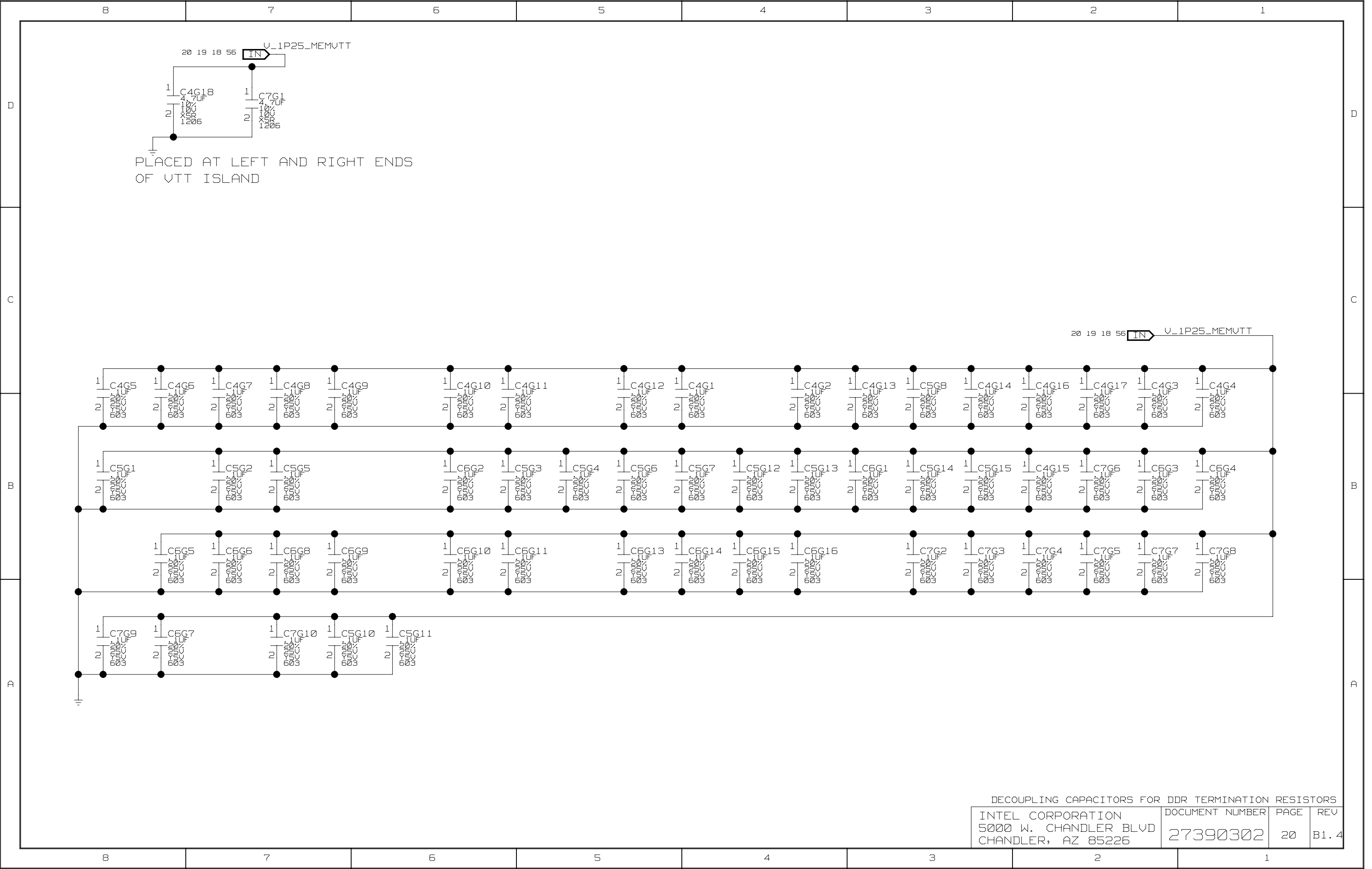


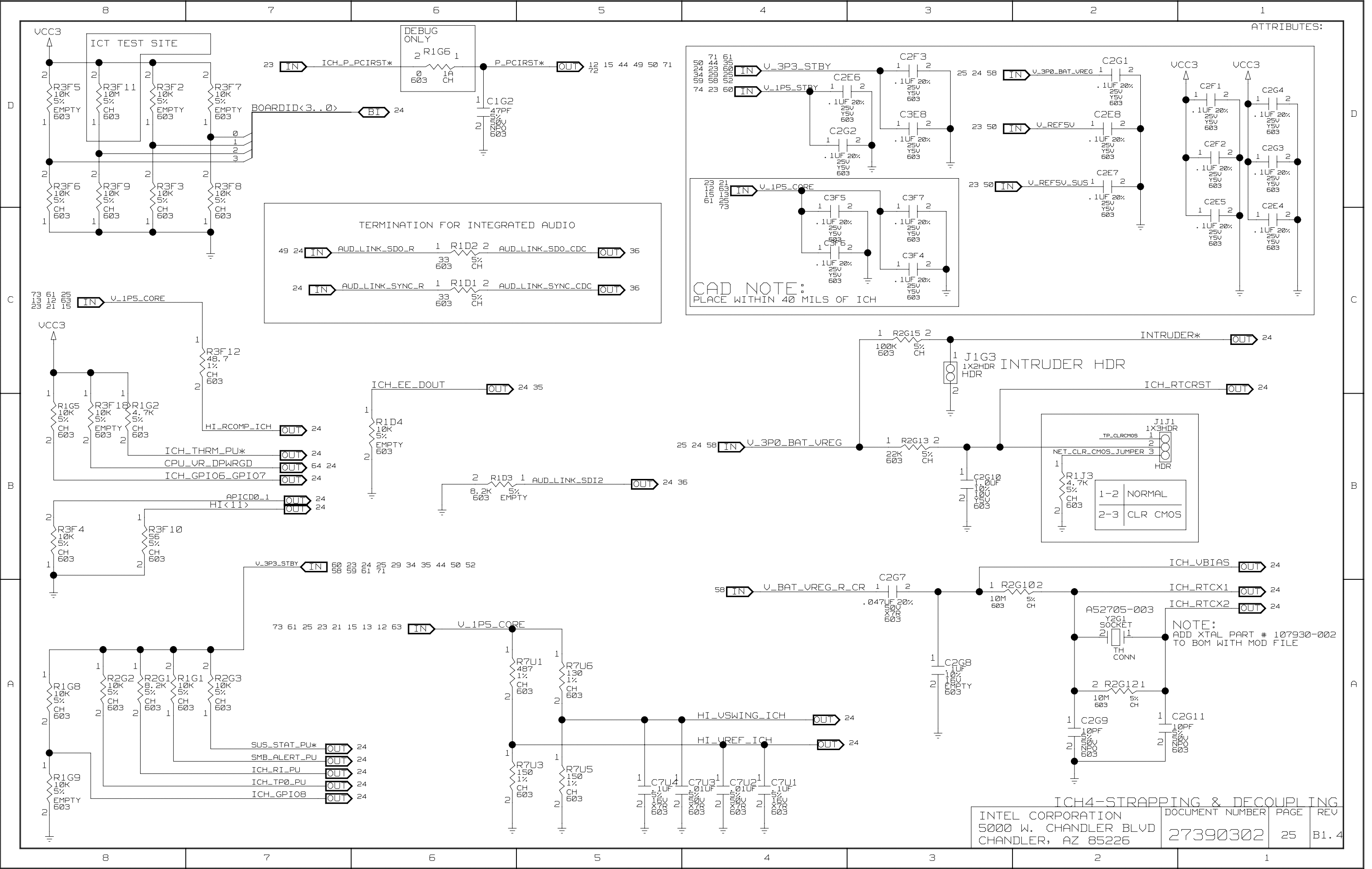




DDR TERMINATION RESISTORS

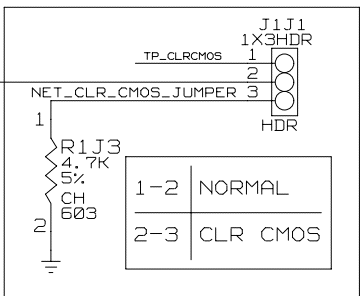
INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 27390302	PAGE 19	REV B1.4
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ATTRIBUTES:

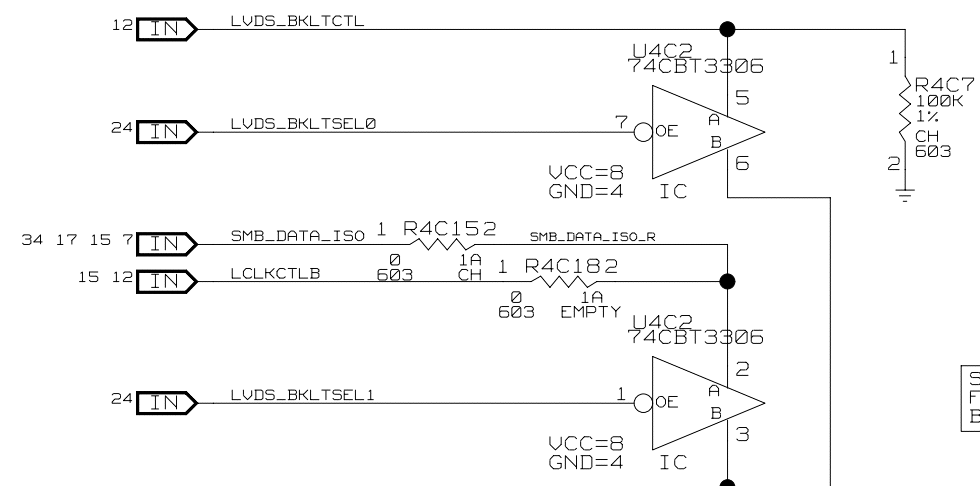
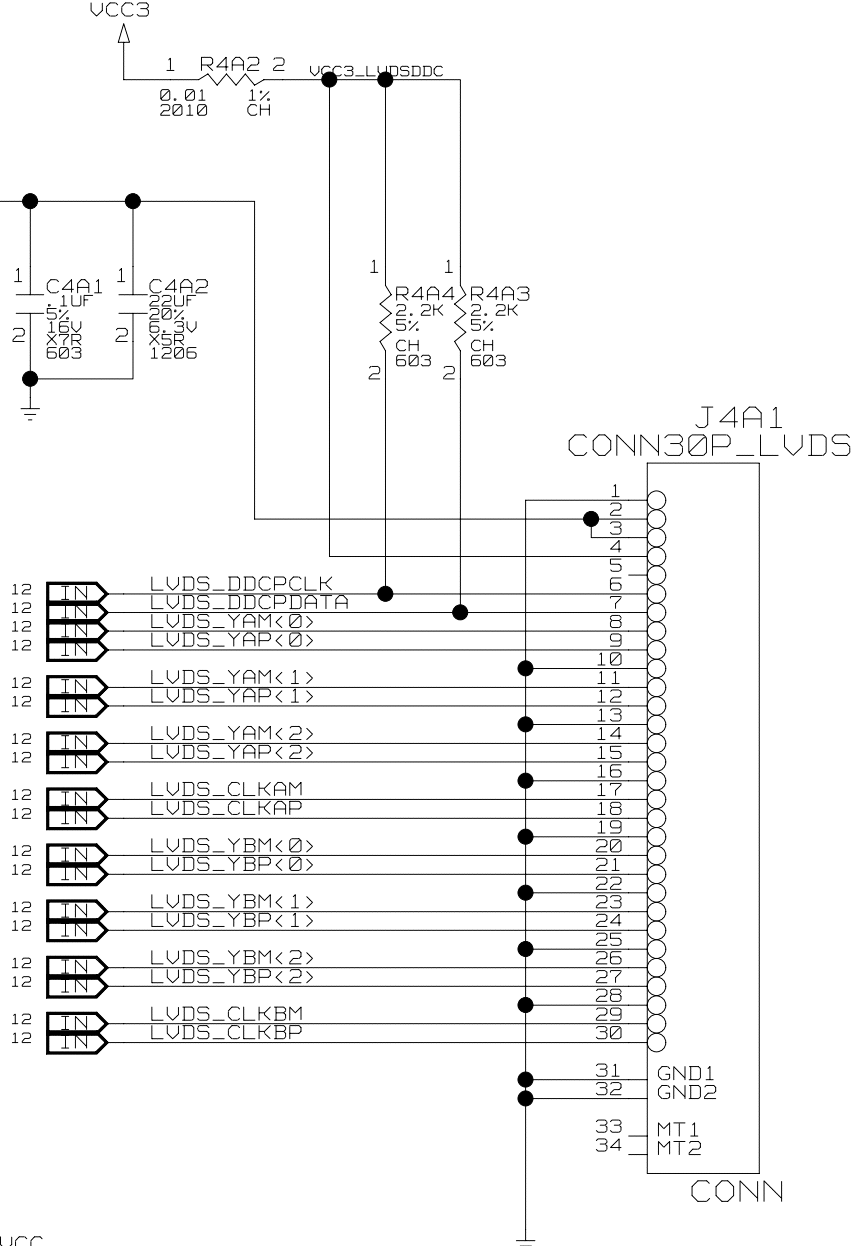
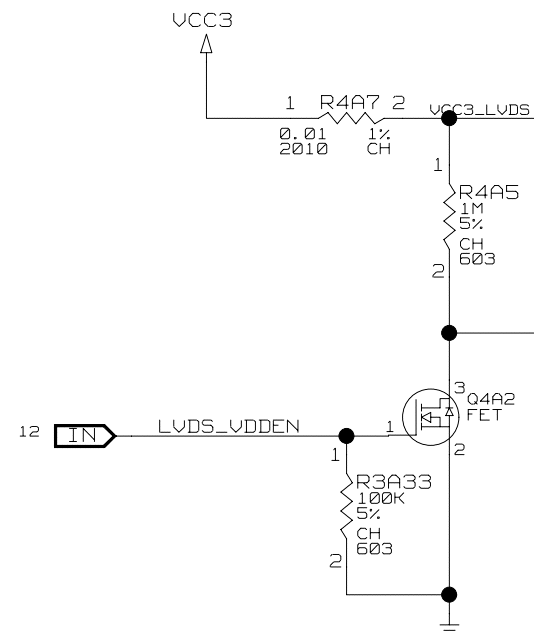
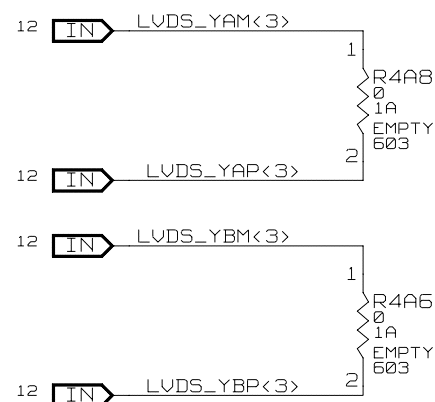
CAD NOTE:
PLACE WITHIN 40 MILS OF ICH



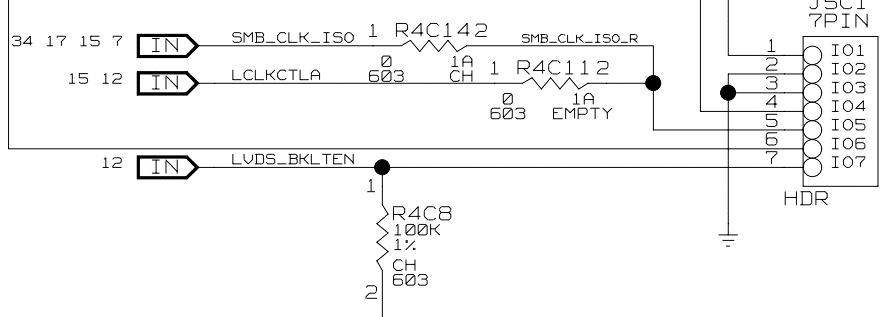
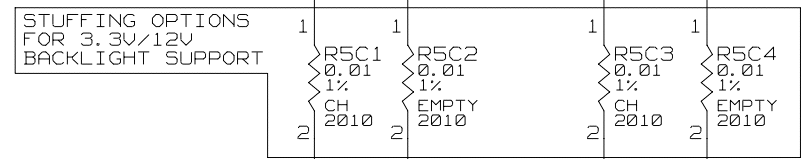
NOTE:
ADD XTAL PART # 107930-002
TO BOM WITH MOD FILE

ICH4-STRAPPING & DECOUPLING

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	27390302	25	B1.4



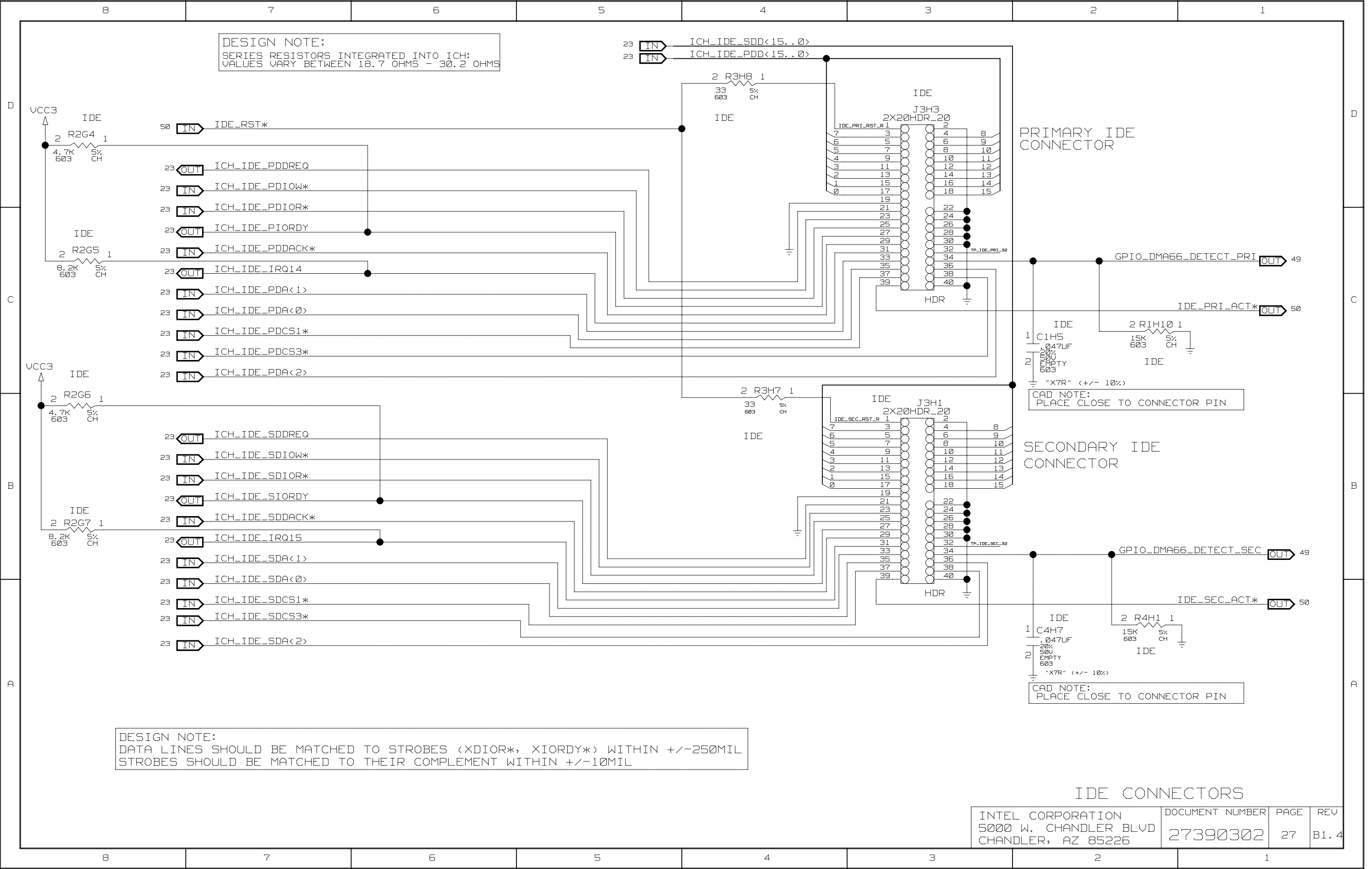
LVDS PANEL BACKLIGHT

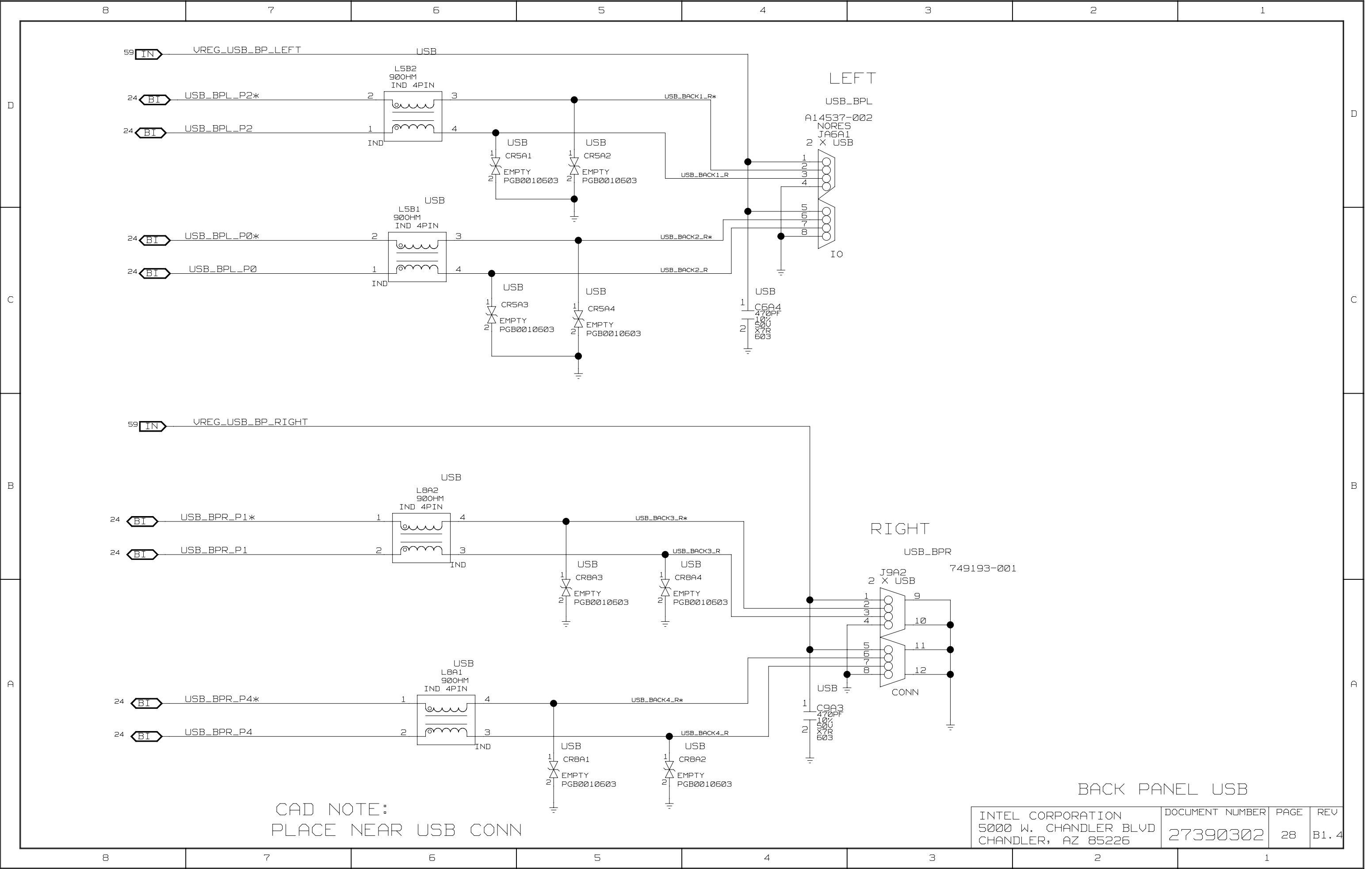


BIOS NOTE:
DISABLE BOTH BKLTSEL
LINES BEFORE ENABLING ONE

LVDS CONNECTOR

INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
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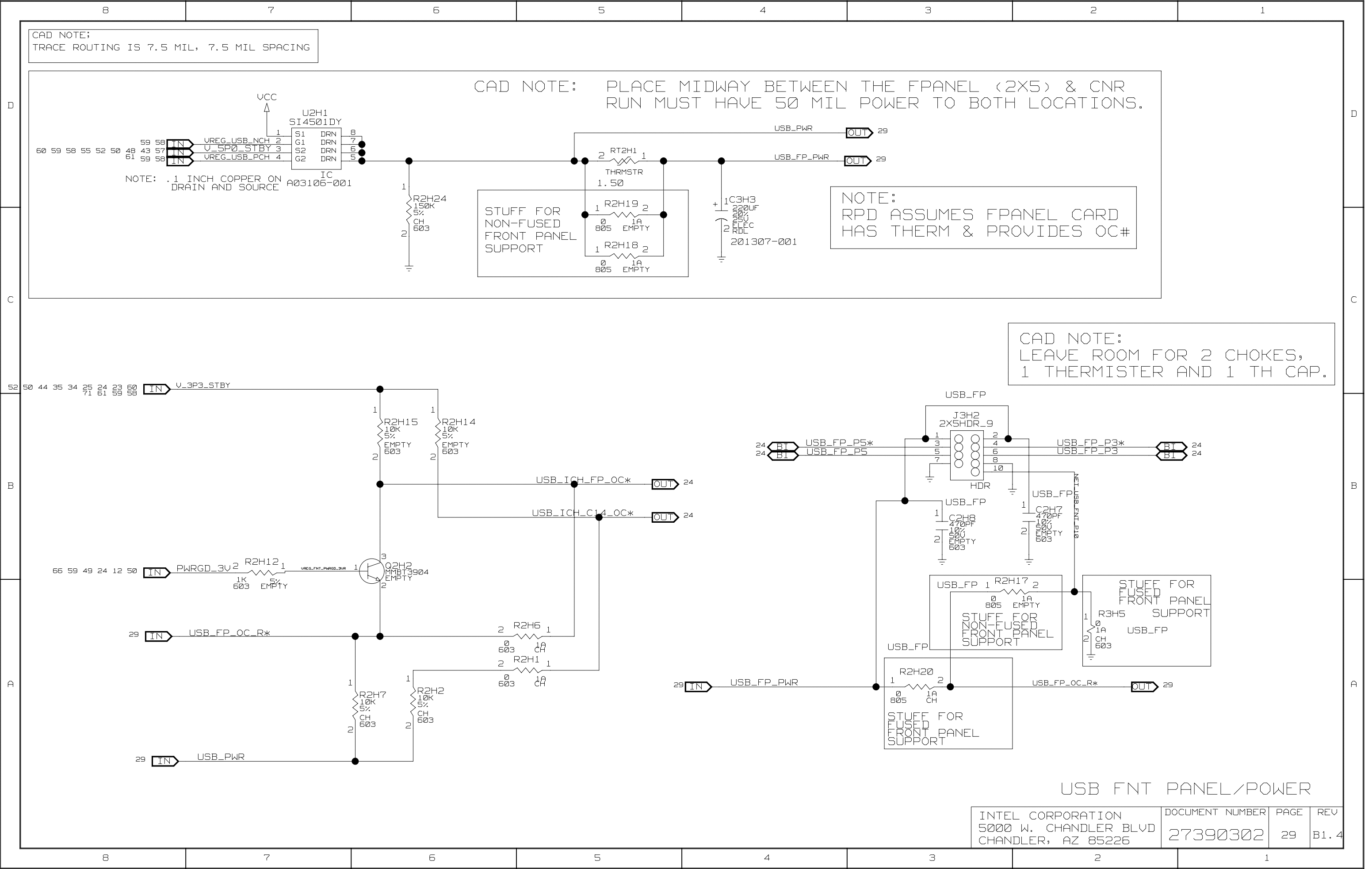


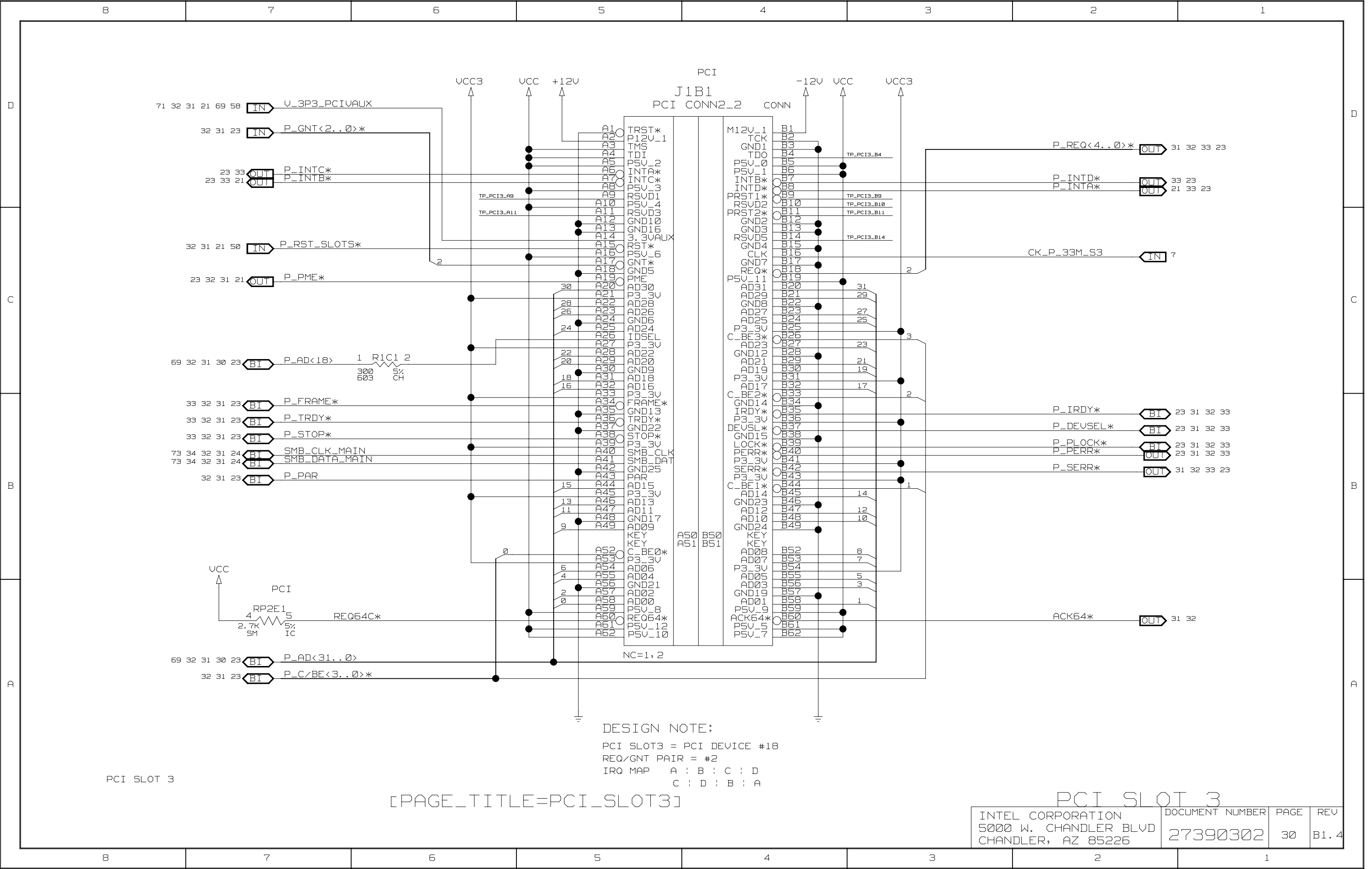


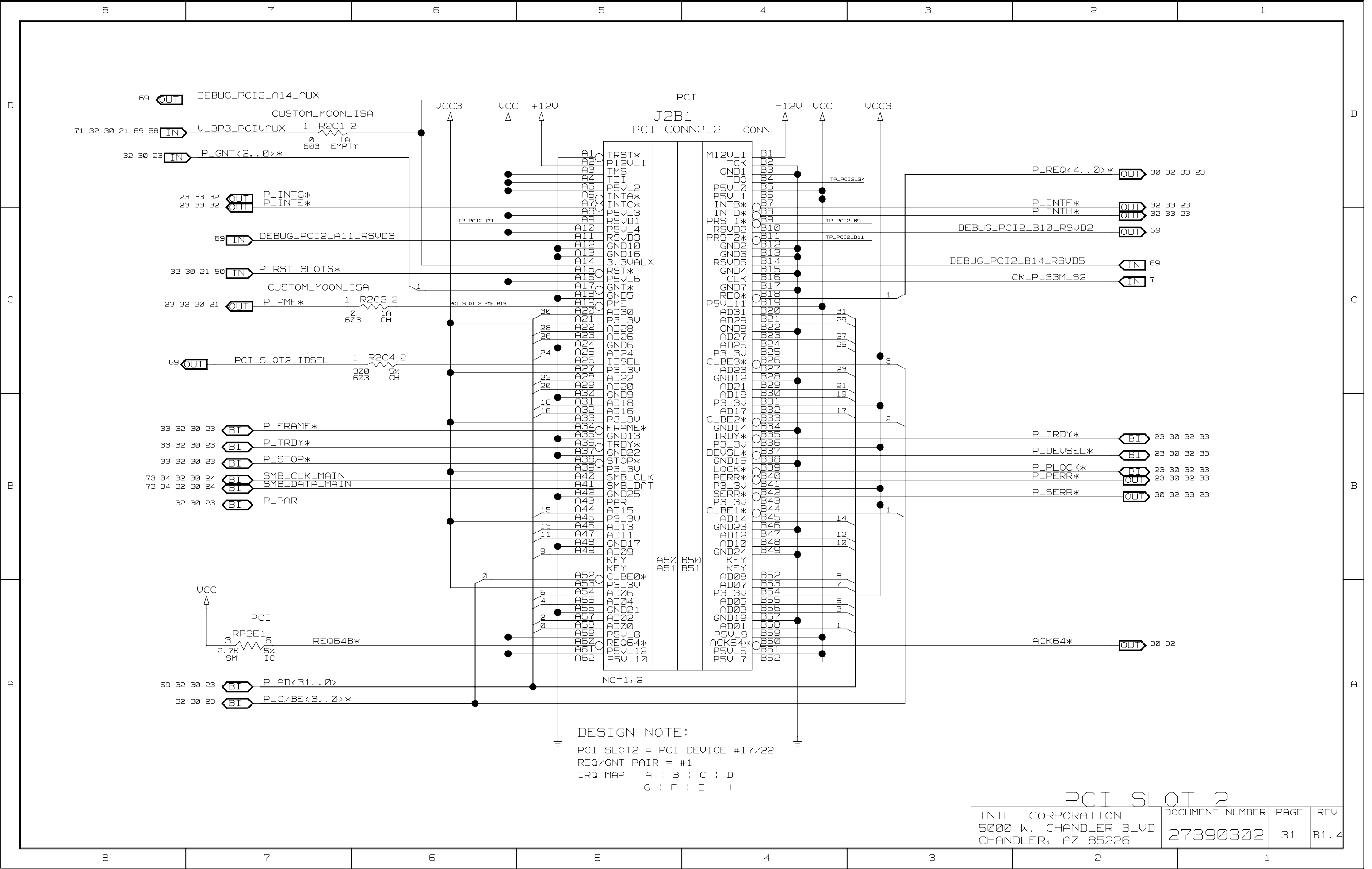
CAD NOTE:
PLACE NEAR USB CONN

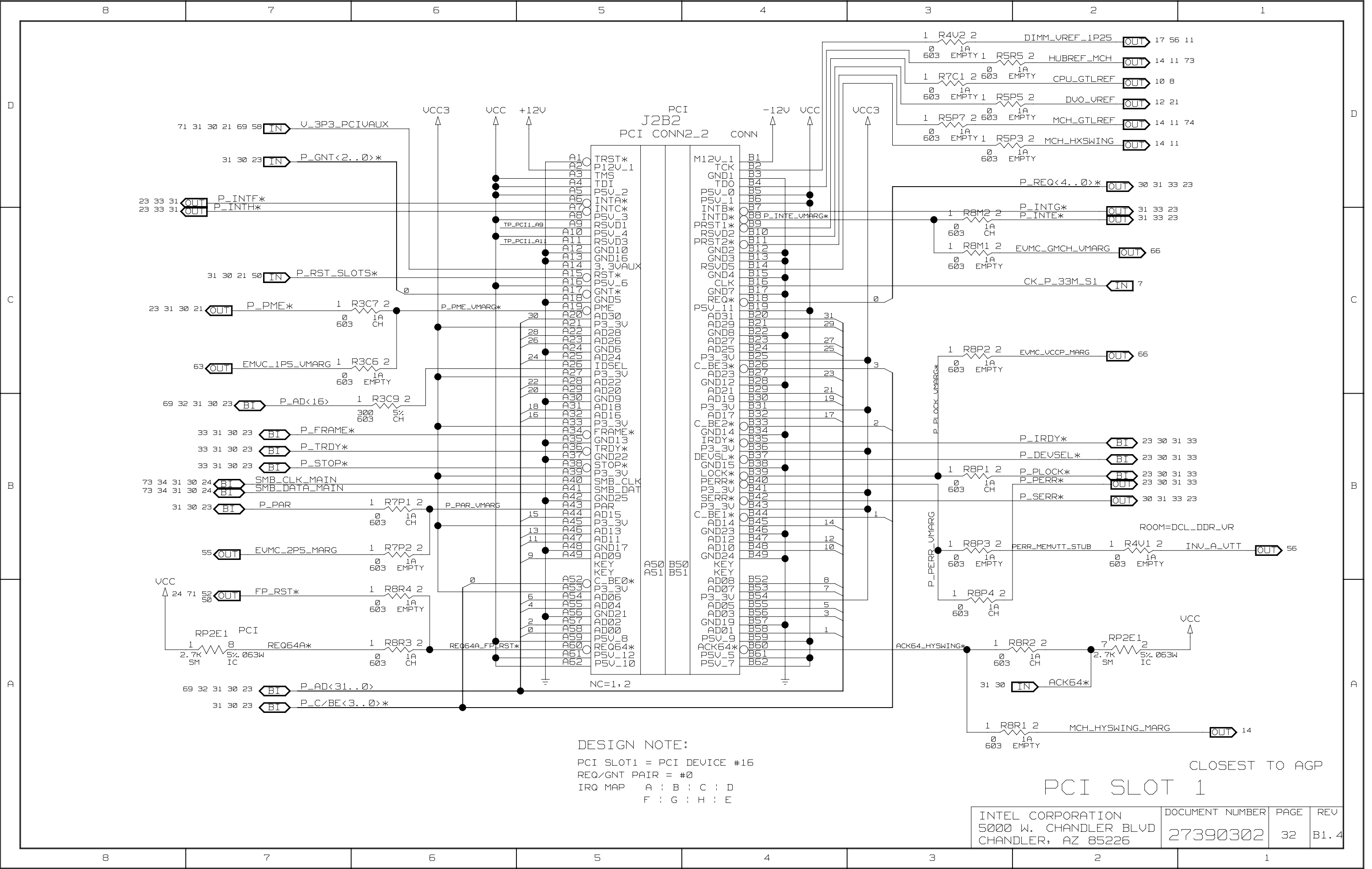
BACK PANEL USB

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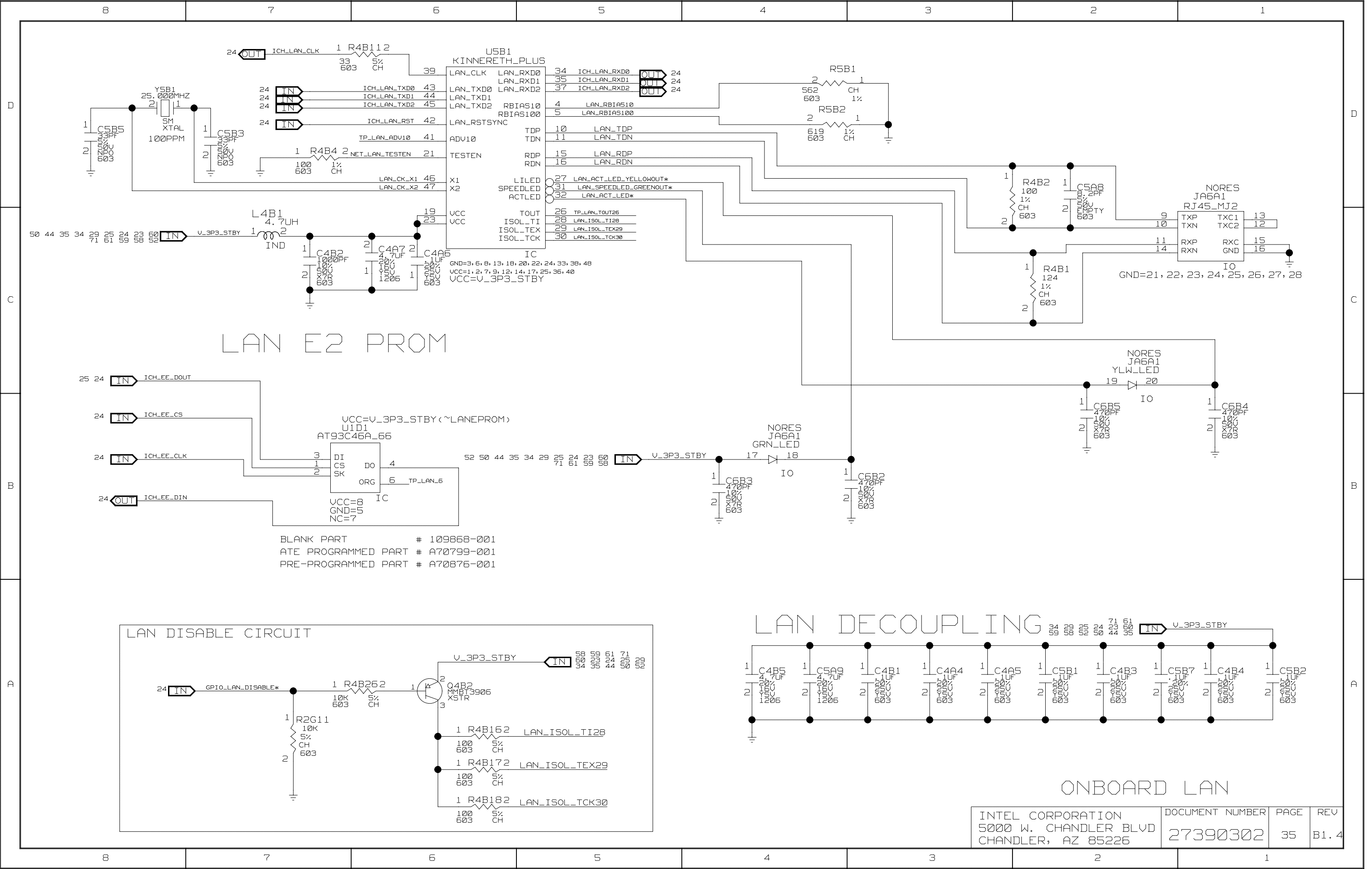
DESIGN NOTE:

PCI SLOT1 = PCI DEVICE #16
REQ/GNT PAIR = #0
IRQ MAP A : B : C : D
 F : G : H : E

CLOSEST TO AGP

PCI SLOT 1

INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 27390302	PAGE 32	REV B1.4
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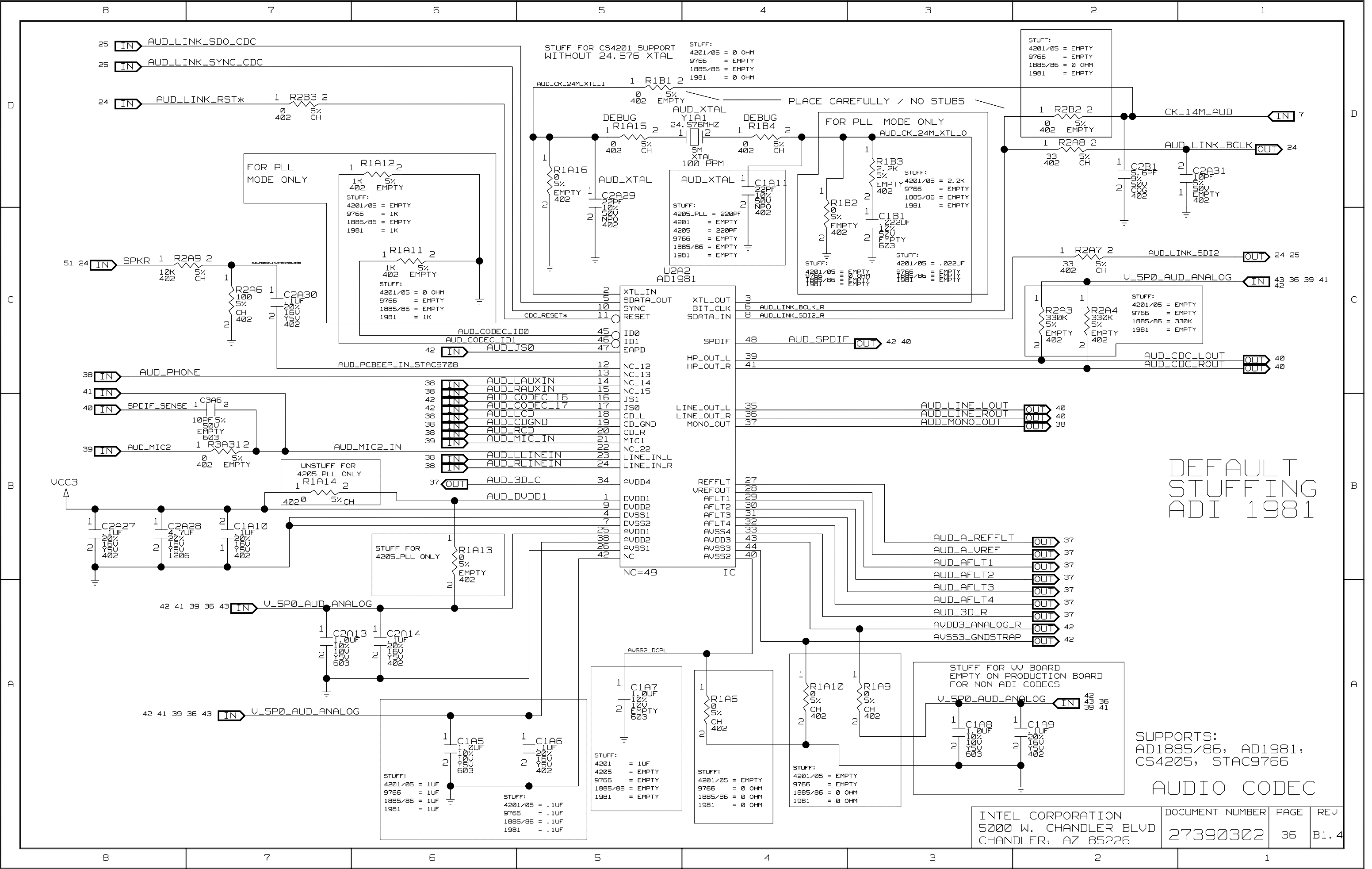
LAN E2 PROM

LAN DECOUPLING

ONBOARD LAN

LAN DISABLE CIRCUIT

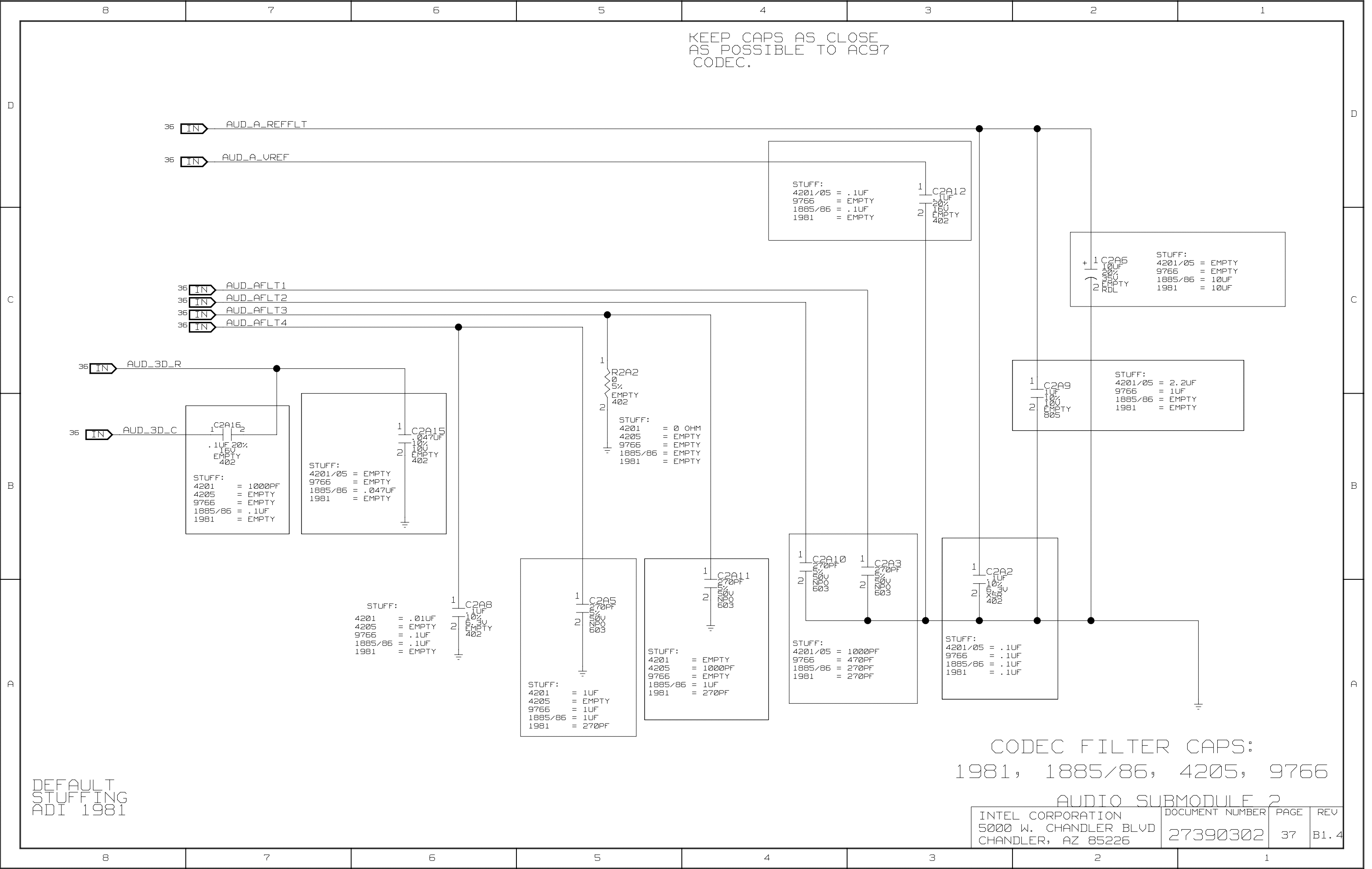
INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 27390302	PAGE 35	REV B1.4
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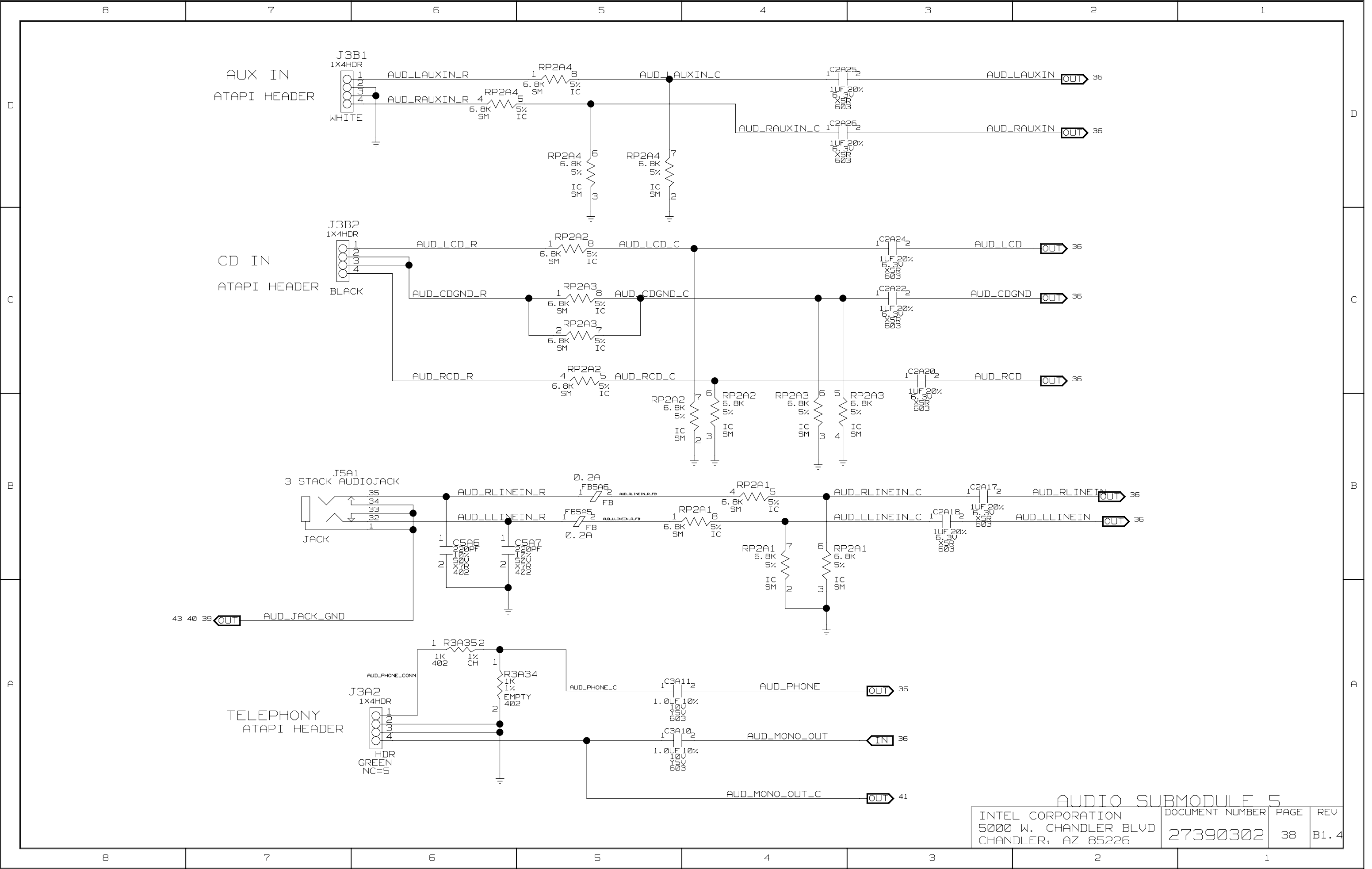


DEFAULT
STUFFING
ADI 1981

SUPPORTS:
AD1885/86, AD1981,
CS4205, STAC9766

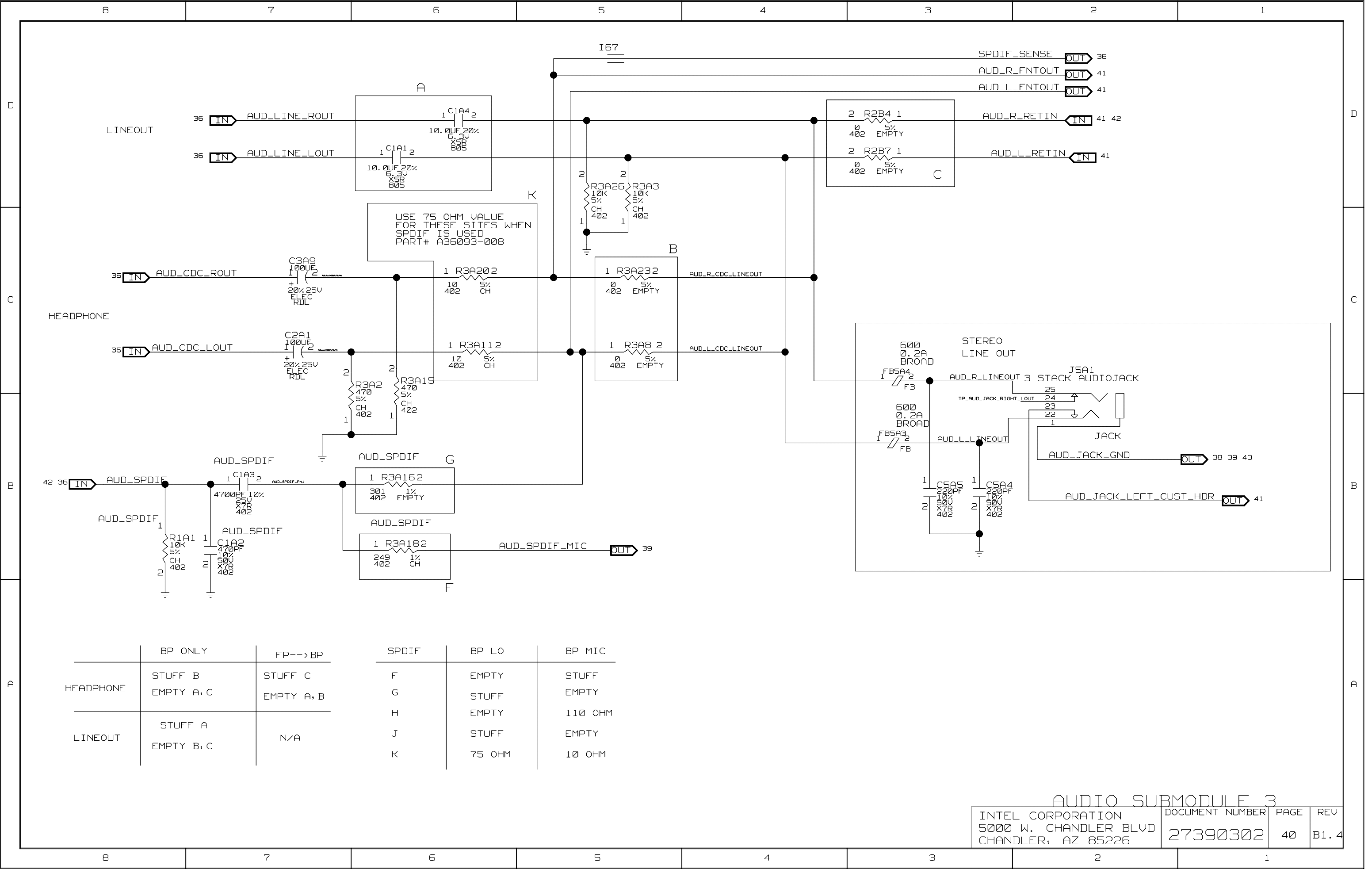
AUDIO CODEC





AUDIO SUBMODULE 5

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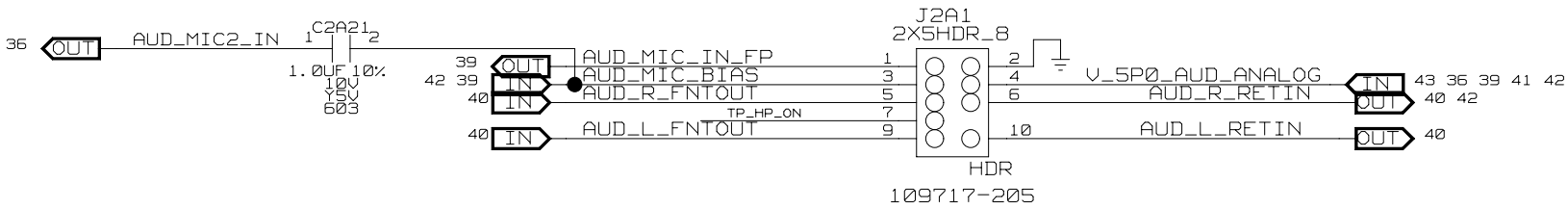
	BP ONLY	FP-->BP	SPDIF	BP LO	BP MIC
HEADPHONE	STUFF B	STUFF C	F	EMPTY	STUFF
	EMPTY A, C	EMPTY A, B	G	STUFF	EMPTY
			H	EMPTY	110 OHM
LINEOUT	STUFF A		J	STUFF	EMPTY
	EMPTY B, C	N/A	K	75 OHM	10 OHM

AUDIO SUBMODULE 3

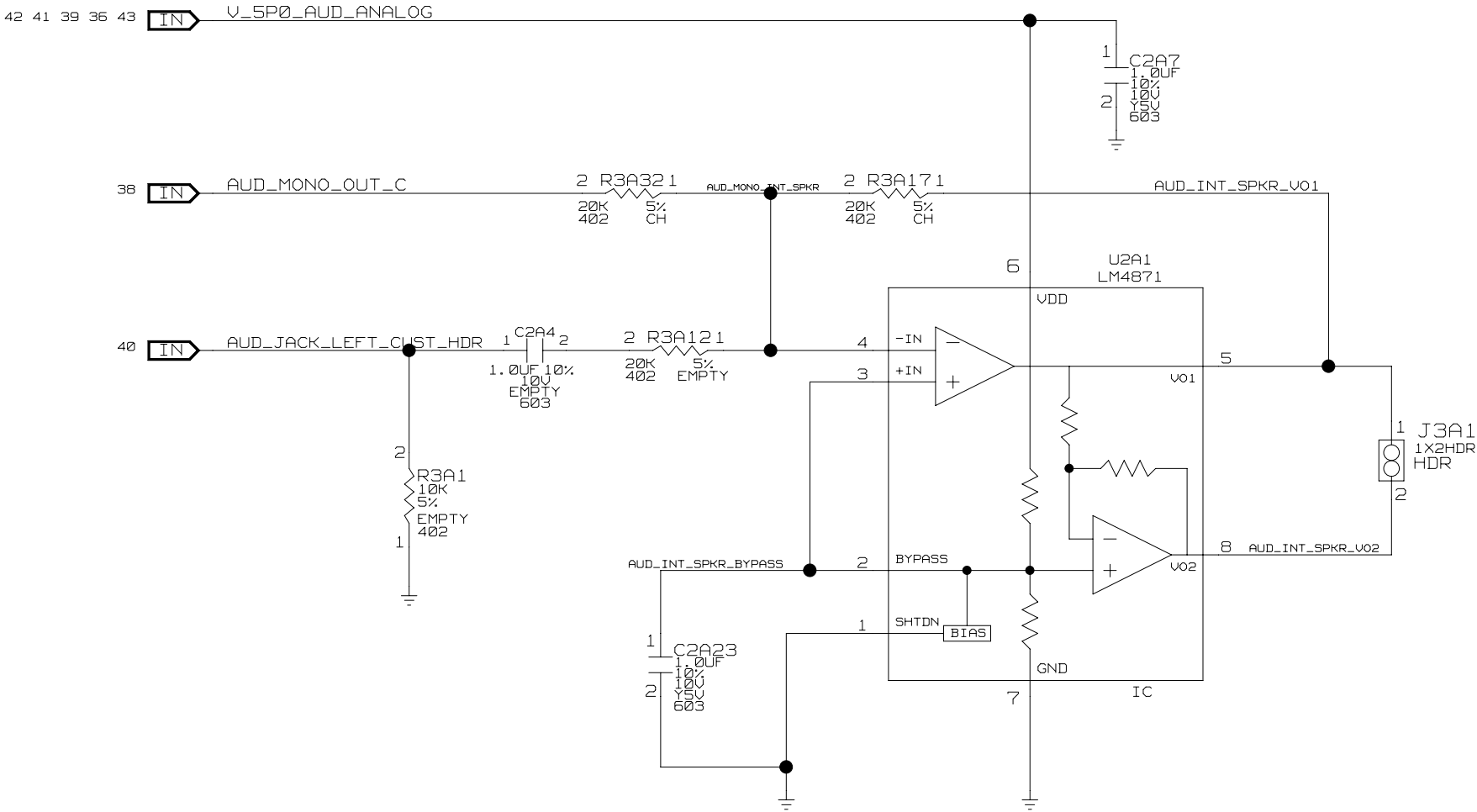
INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 27390302	PAGE 40	REV B1.4
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NOTE:
FP DONGLE MUST HAVE
MIC JACK RING SHUNT SPRING
TERMINAL CONNECTED
TO GND FOR PROPER
MIC SENSING OPERATION

PLACE NEAR AUDIO CIRCUIT



INTERNAL SPEAKER CIRCUIT



AUDIO FRONT PANEL

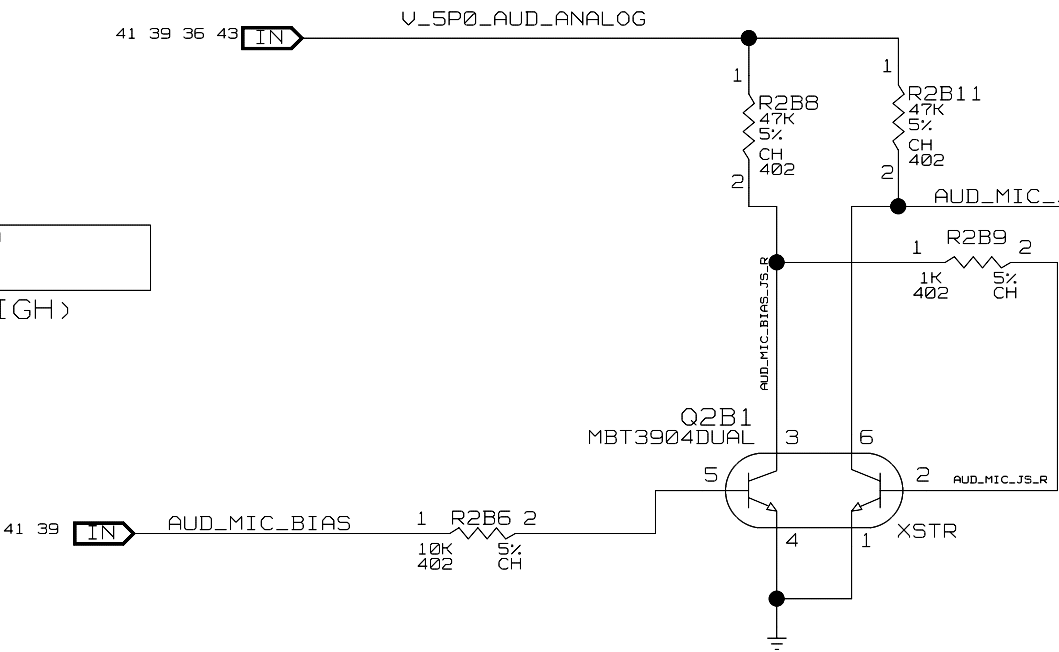
INTEL CORPORATION	DOCUMENT NUMBER	PAGE	REV
5000 W. CHANDLER BLVD CHANDLER, AZ 85226	27390302	41	B1.4

MIC JACK SENSE NOTE:

FP DONGLE MUST HAVE
MIC JACK RING SHUNT SPRING
TERMINAL CONNECTED
TO GND FOR PROPER
MIC SENSING OPERATION

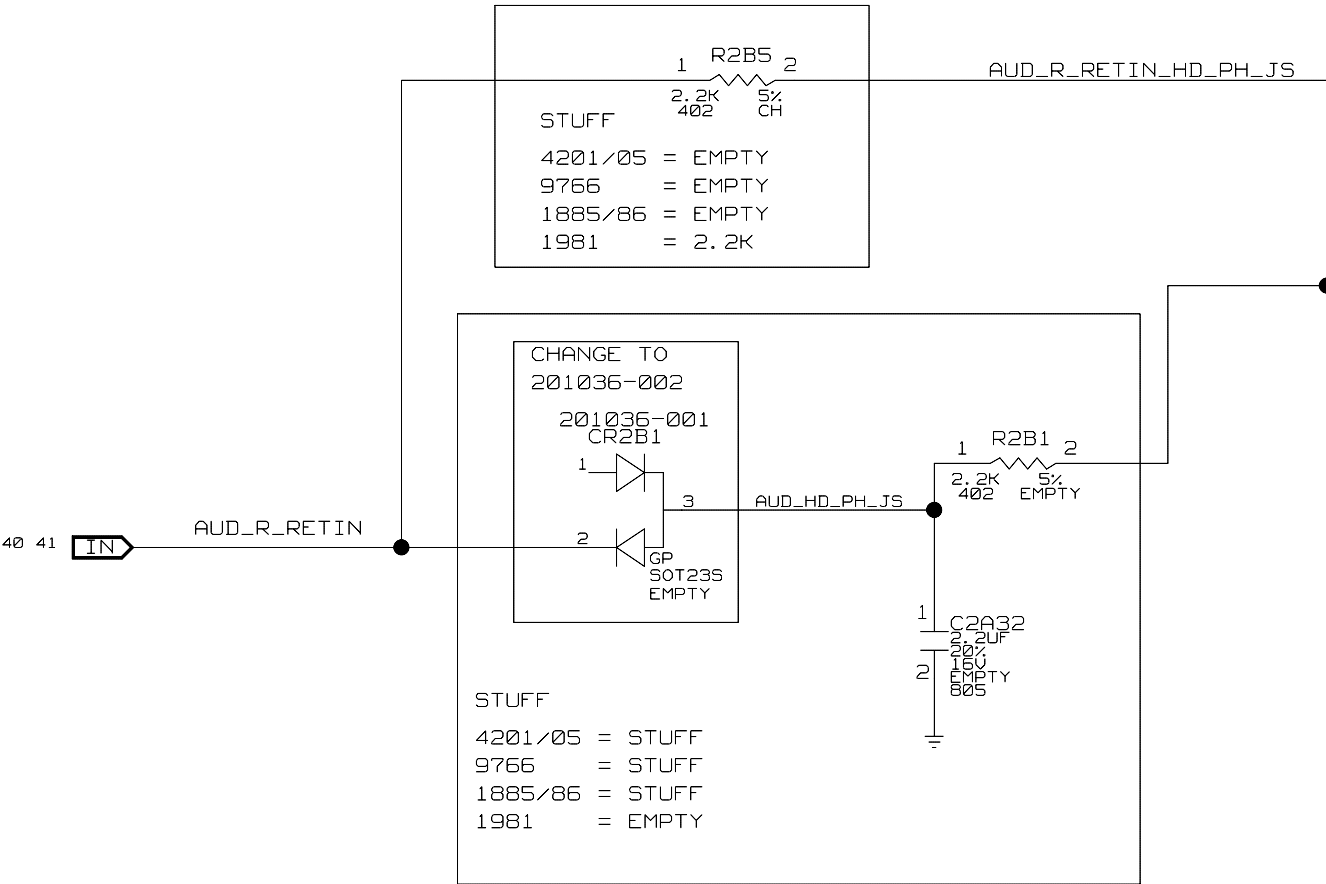
GPIO LOCATIONS:

4205: 43, 44, 41, 40, 39
1981: 16, 17 (ACTIVE HIGH)
9766: 43, 44
4291: NONE
1885/86: 47, 48



NOTE:
TOP RESISTOR STUFF: 1981
MIDDLE RESISTOR STUFF: 9766/4205
BOTTOM RESISTOR STUFF: 1885/86

HEADPHONE JACK SENSE

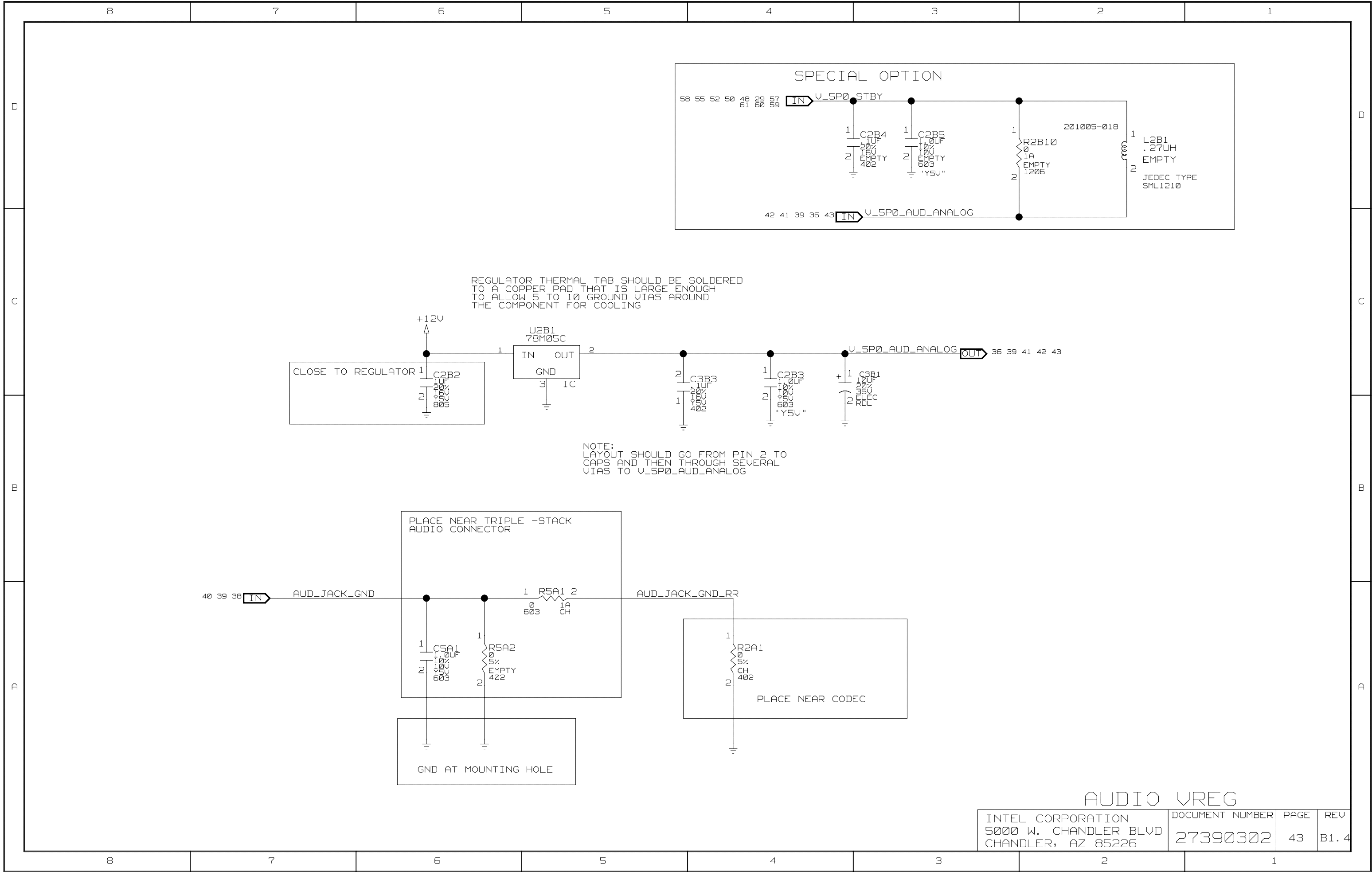


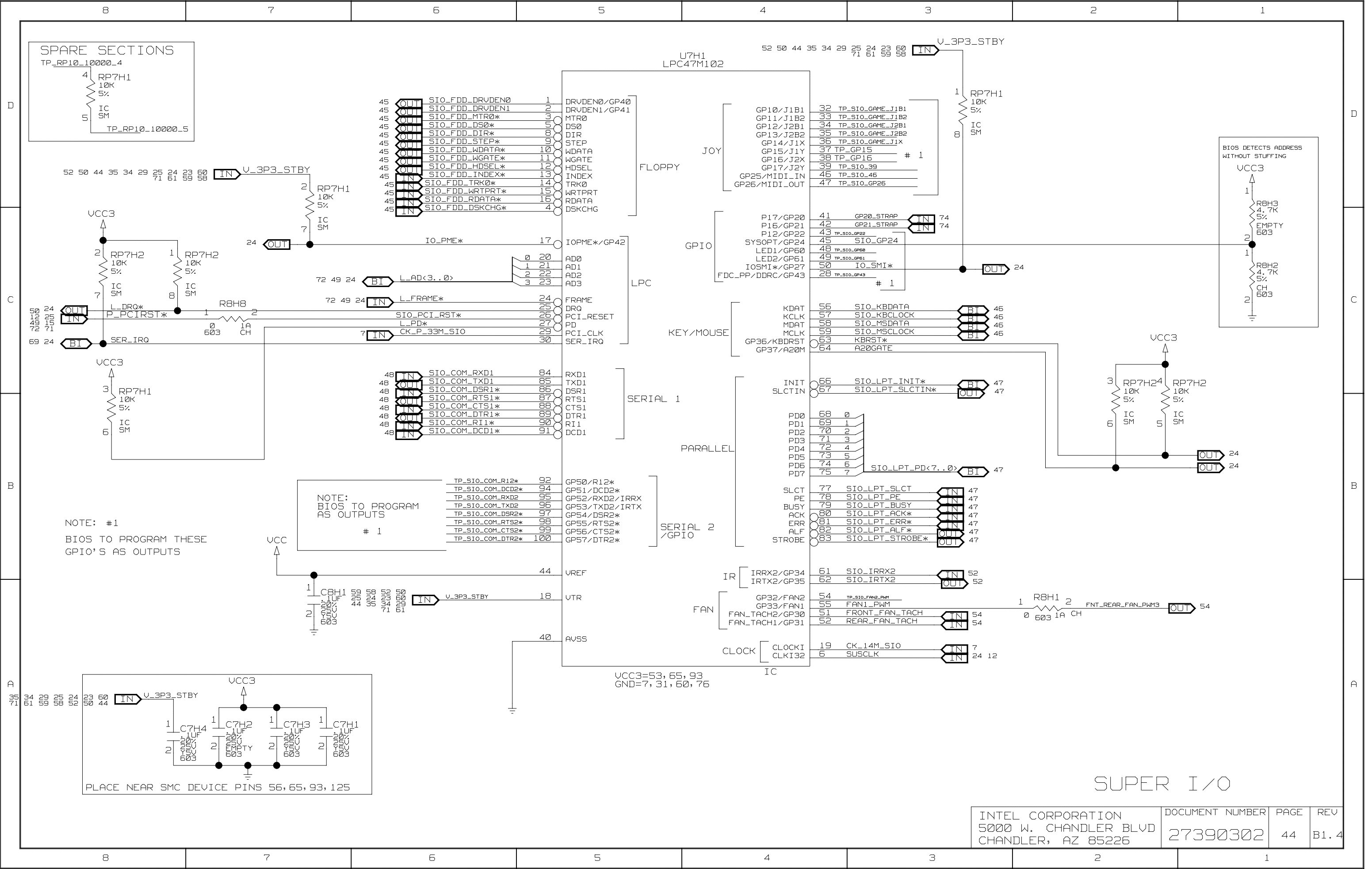
NOTE:
TOP RESISTOR STUFF: 1981
MIDDLE RESISTOR STUFF: 9766/4205
BOTTOM RESISTOR STUFF: 1885/86

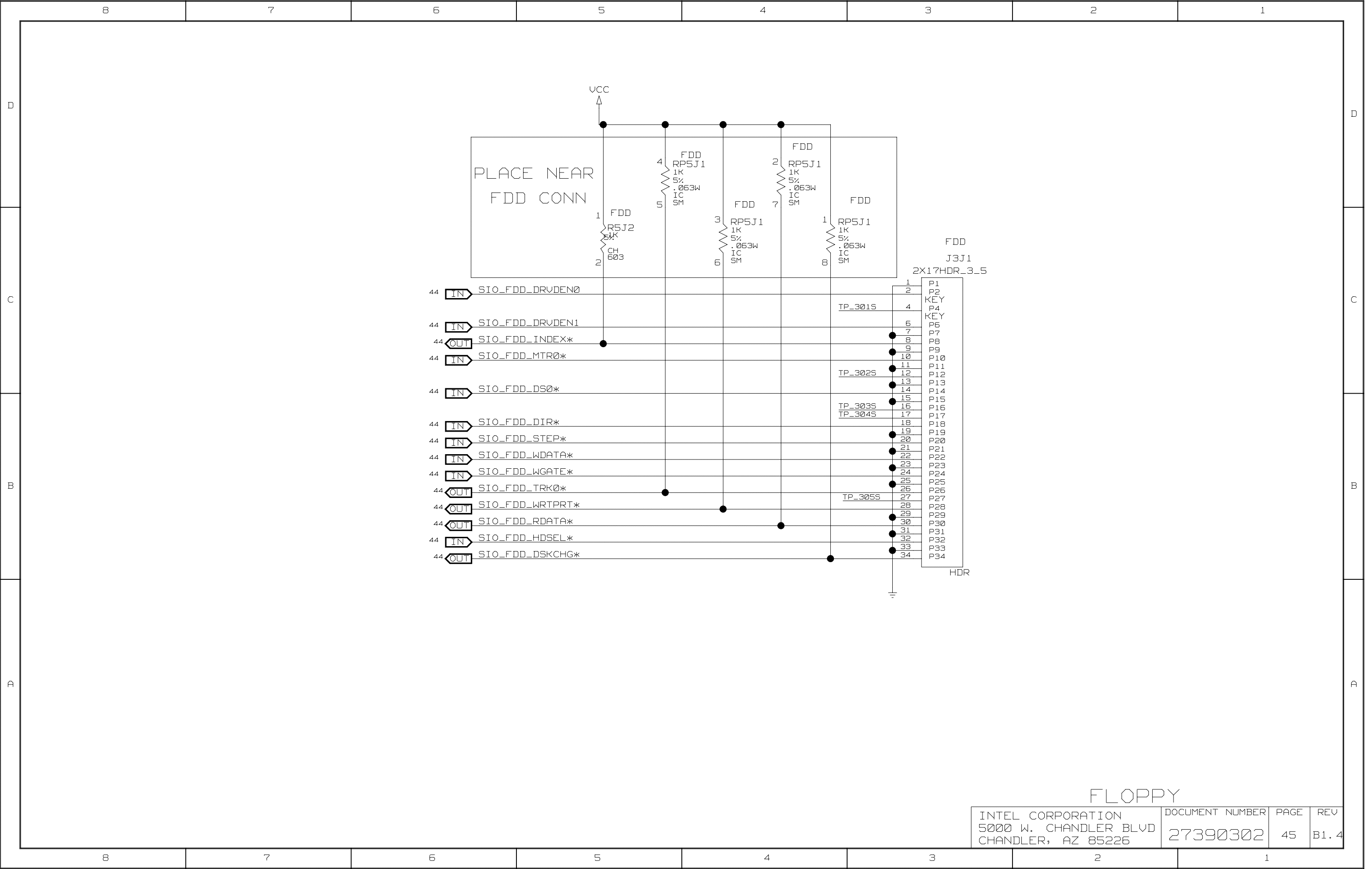
DEFAULT
STUFFING
ADI 1981

MIC/HEADPHONE

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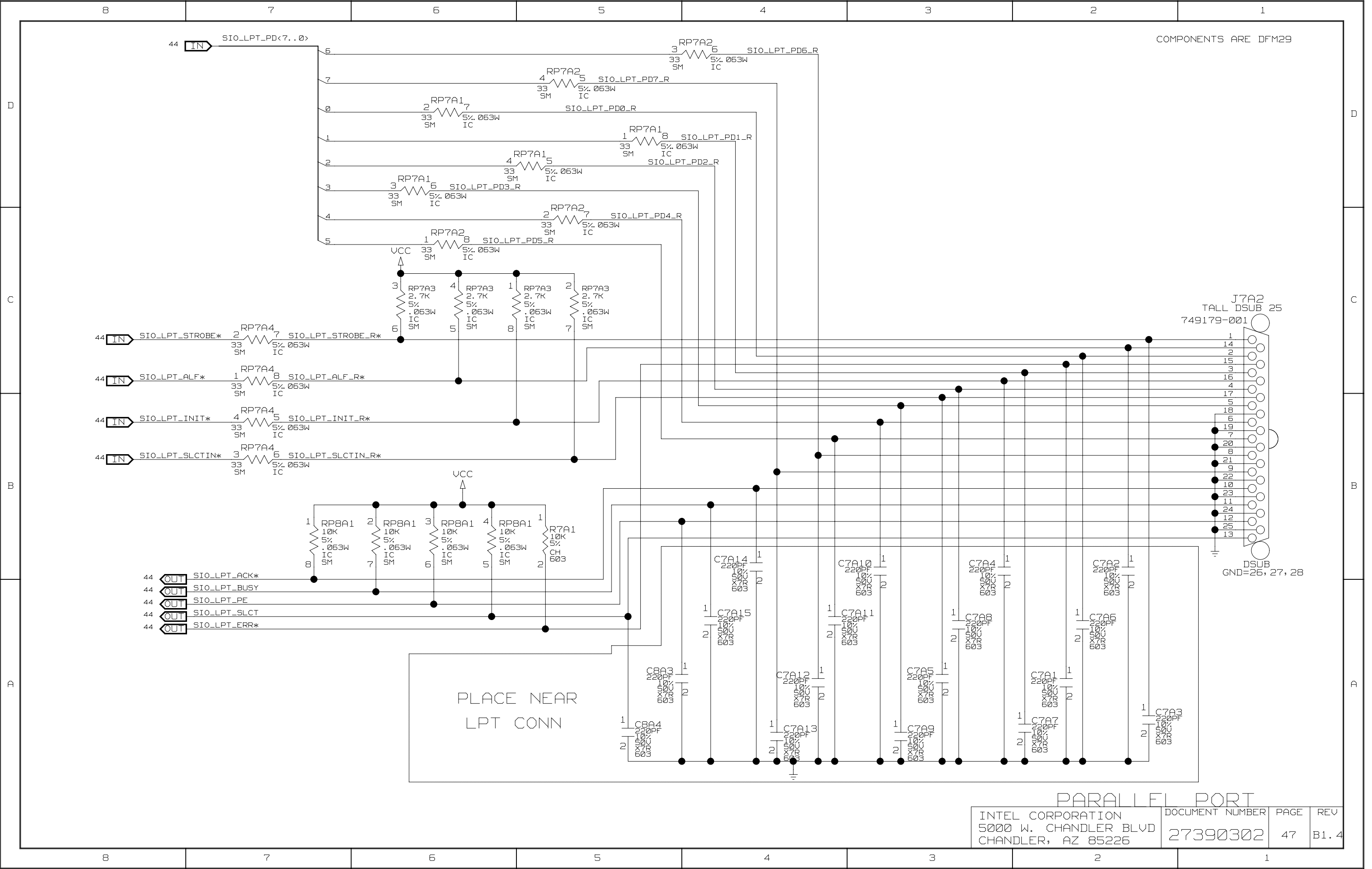






FLOPPY

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COMPONENTS ARE DFM29

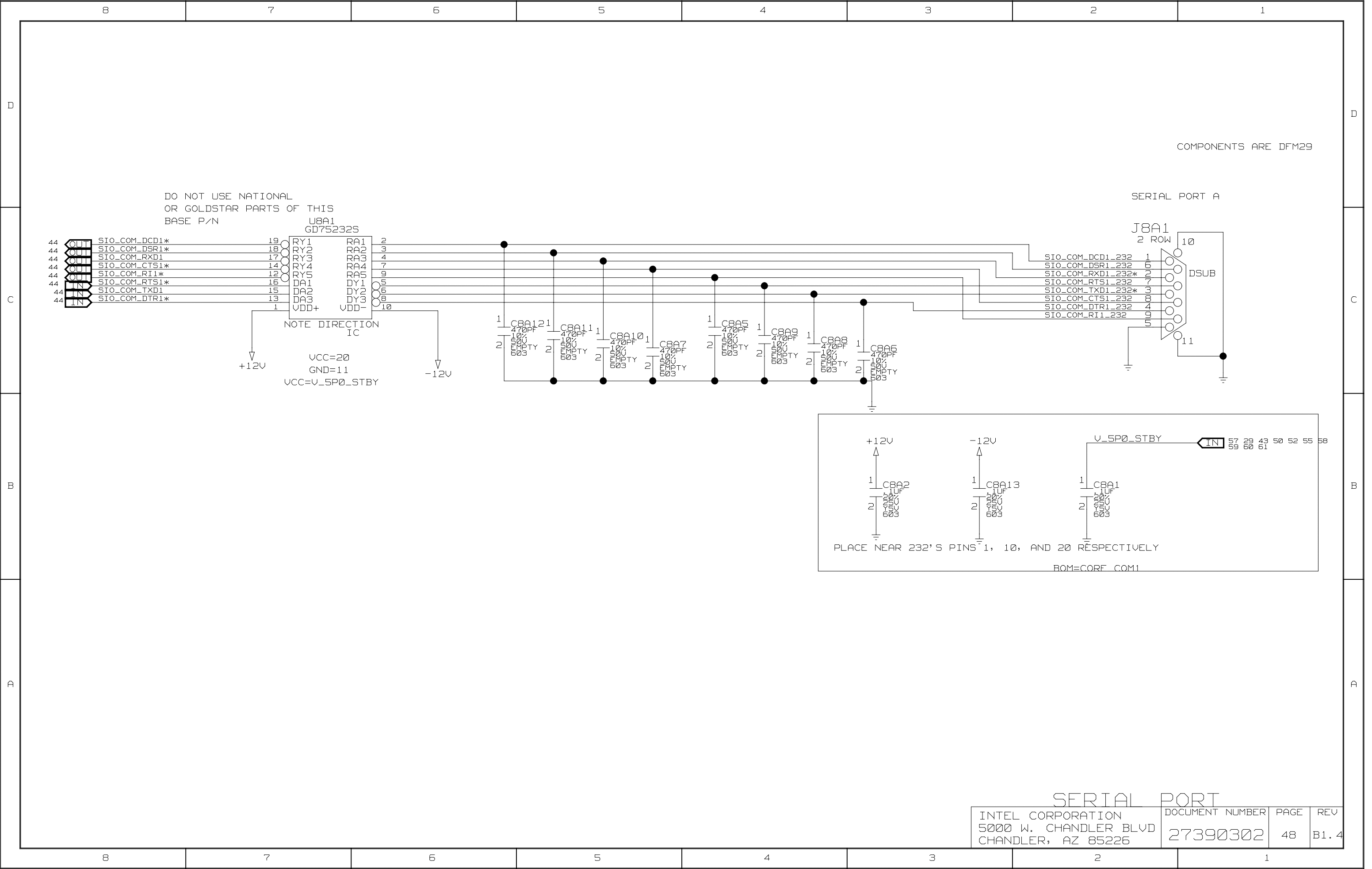
J7A2
TALL DSUB 25
749179-001

DSUB
GND=26, 27, 28

PLACE NEAR
LPT CONN

PARALLEL PORT

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COMPONENTS ARE DFM29

SERIAL PORT A

J8A1

2 ROW

DSUB

NOTE DIRECTION
IC

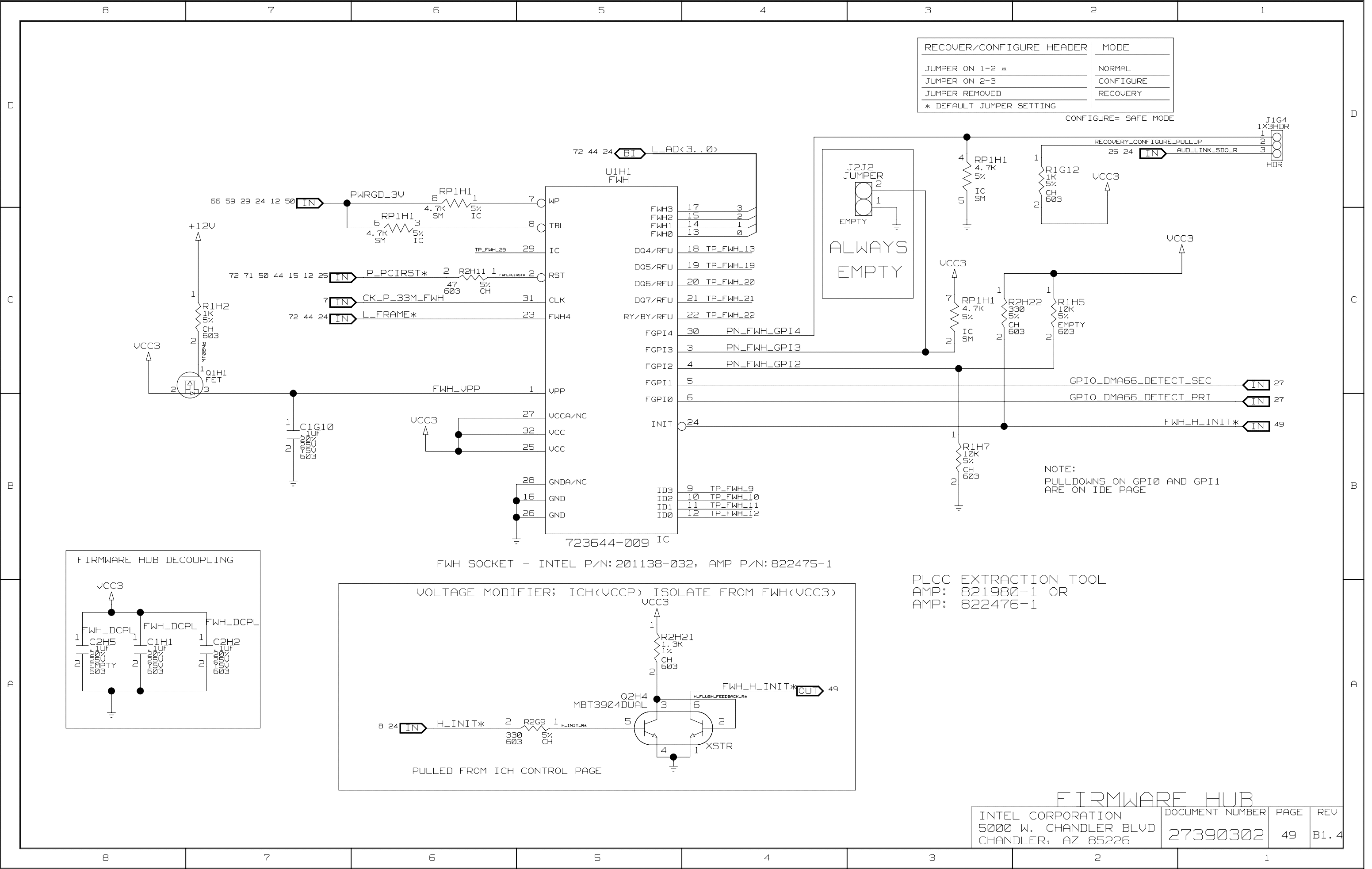
VCC=20
GND=11
VCC=V_5P0_STBY

PLACE NEAR 232'S PINS 1, 10, AND 20 RESPECTIVELY

BOM=CORF COM1

SERIAL PORT

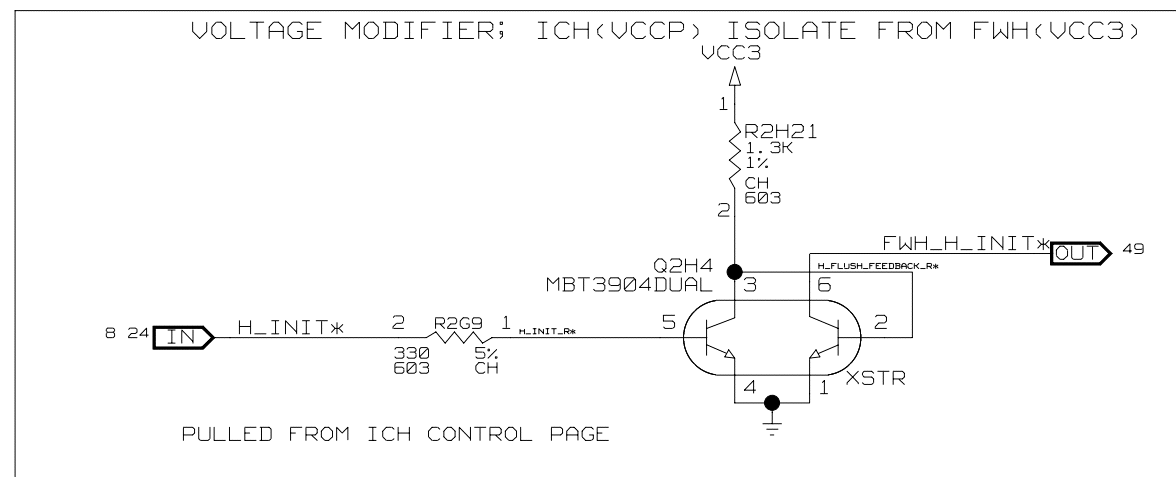
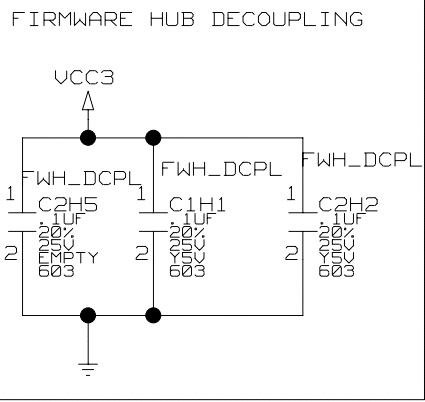
INTEL CORPORATION 5000 W. CHANDLER BLVD CHANDLER, AZ 85226	DOCUMENT NUMBER 27390302	PAGE 48	REV B1.4
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RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

CONFIGURE= SAFE MODE

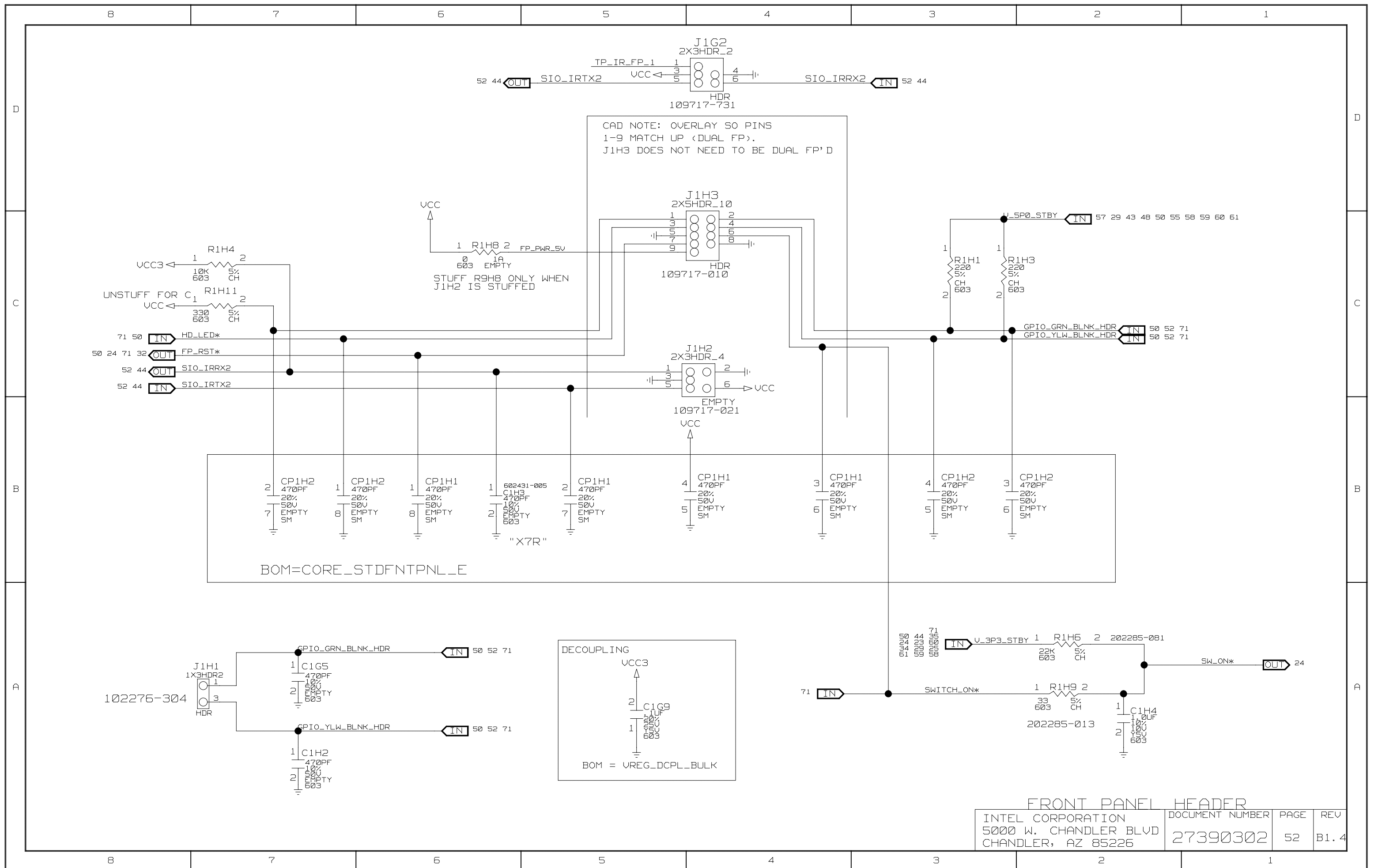
NOTE:
PULLDOWNS ON GPIO AND GPI1
ARE ON IDE PAGE

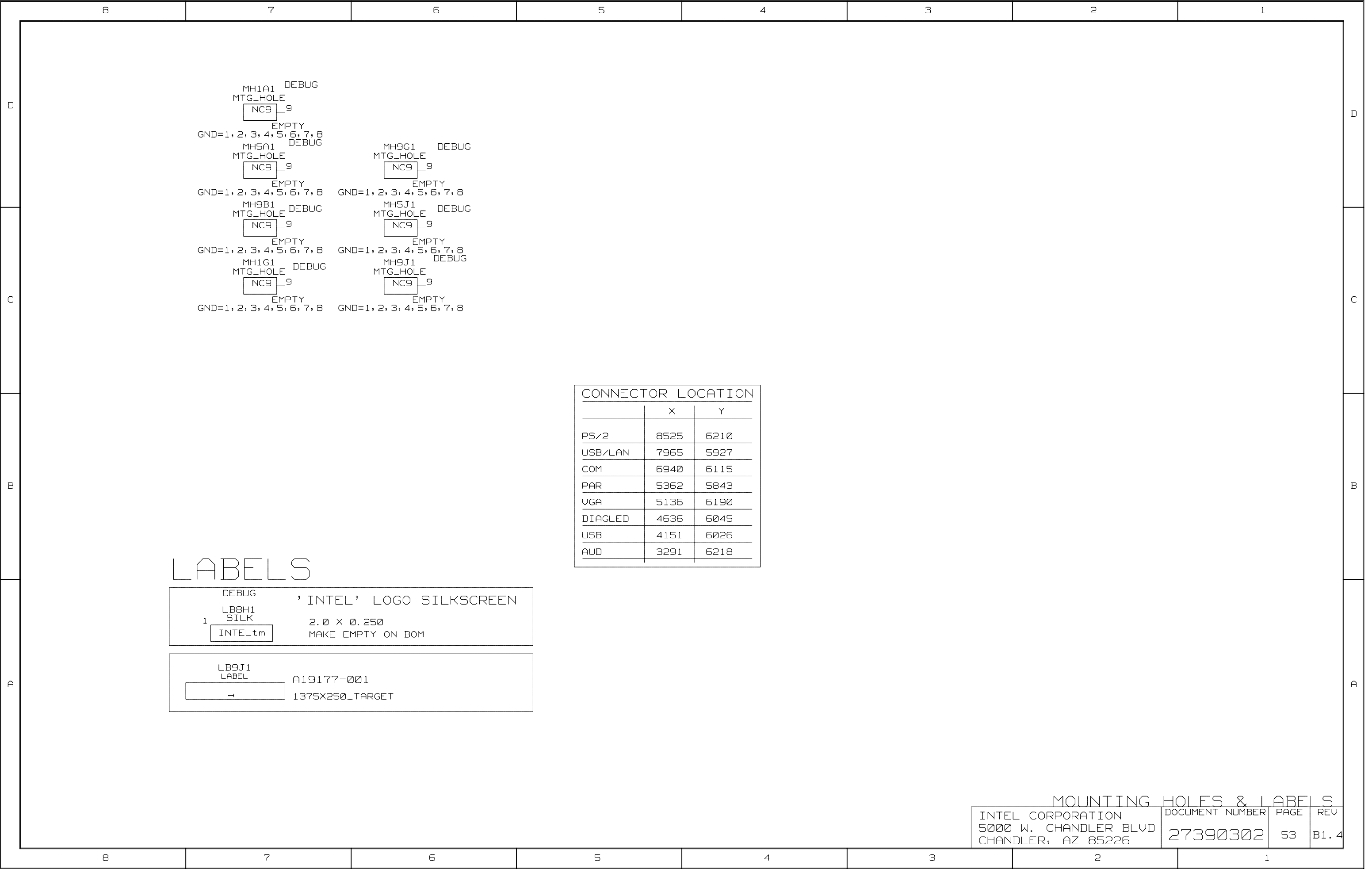


PLCC EXTRACTION TOOL
AMP: 821980-1 OR
AMP: 822475-1

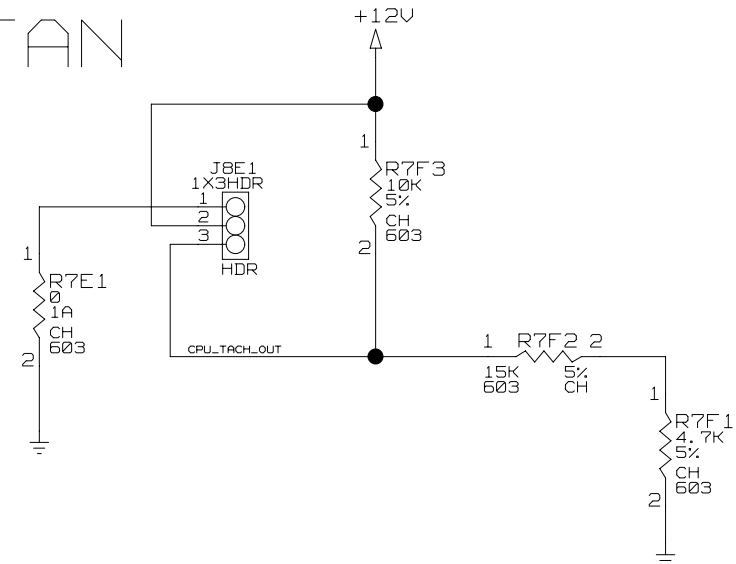
FIRMWARE HUB

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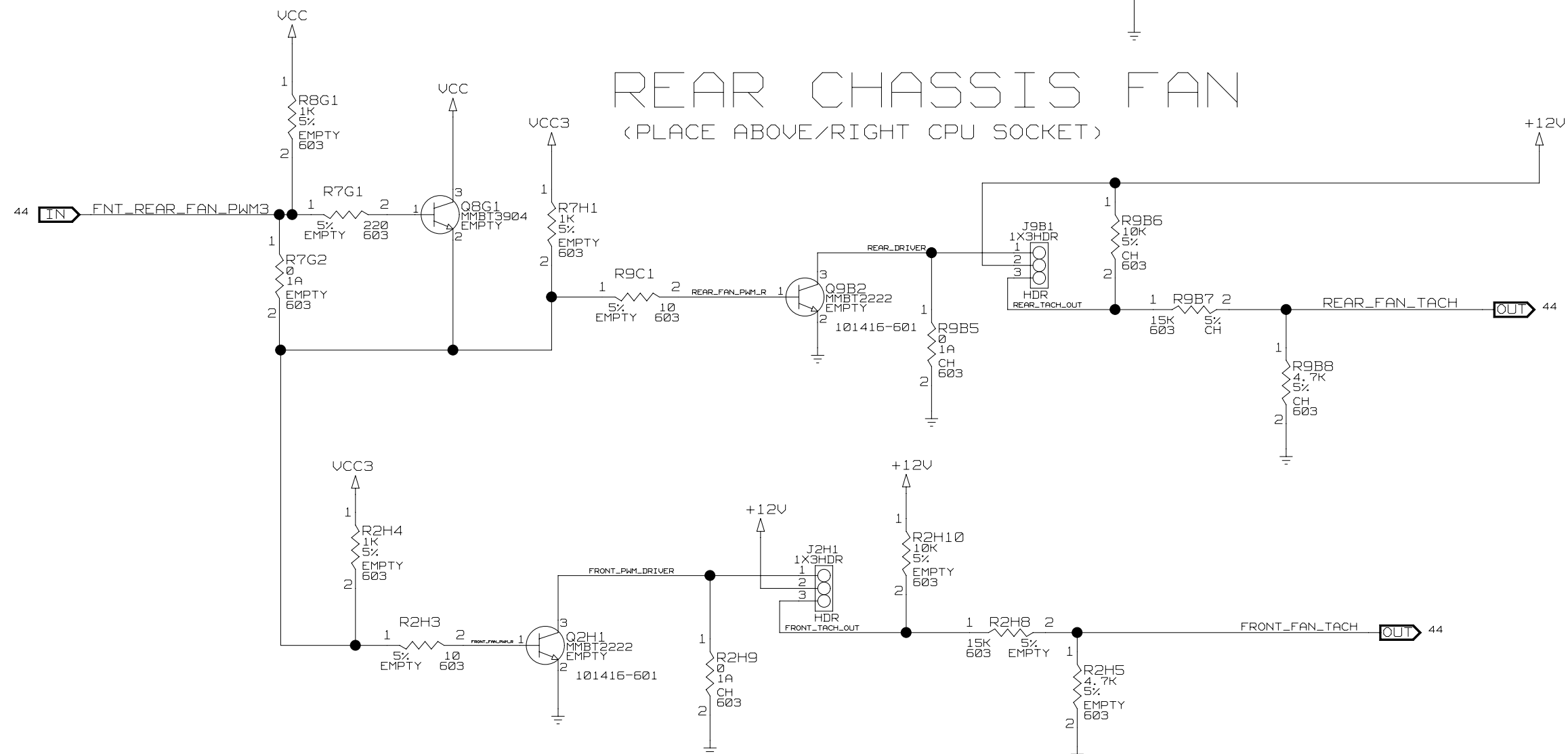




(PLACE BELOW/RIGHT CPU SOCKET)

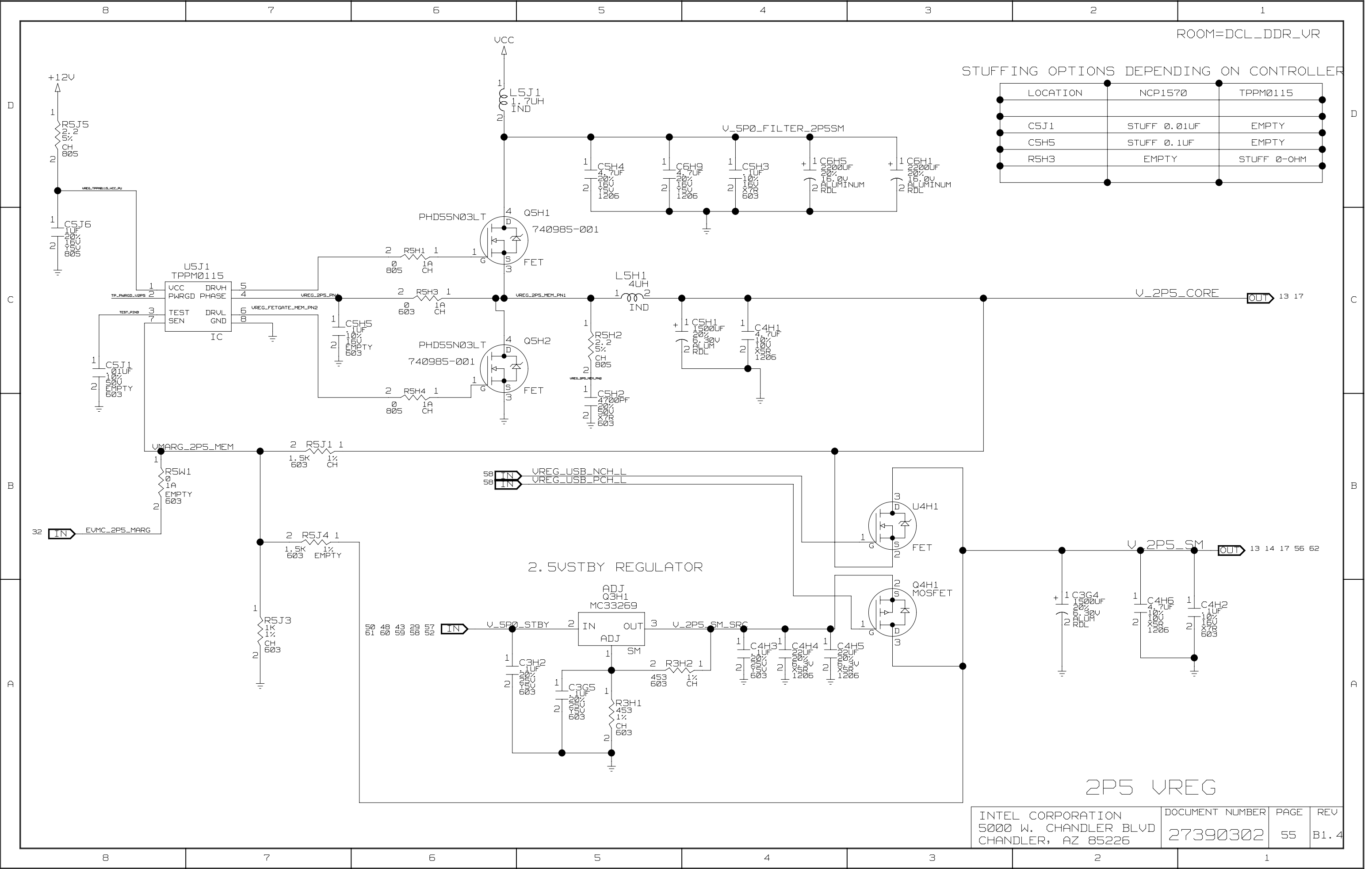


(PLACE ABOVE/RIGHT CPU SOCKET)



(PLACE LOWER LEFT CORNER OF PLATFORM)

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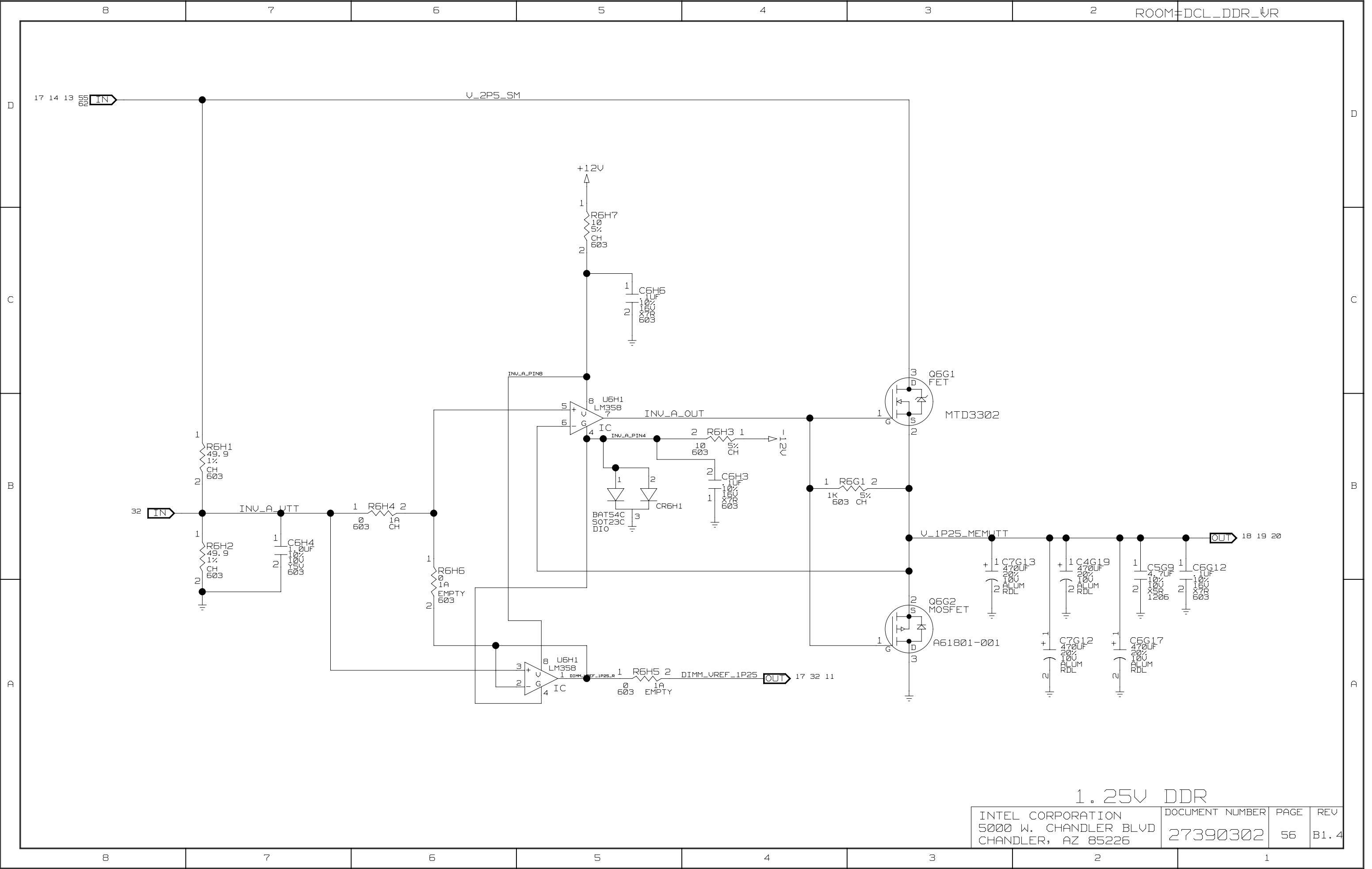
ROOM=DCL_DDR_VR

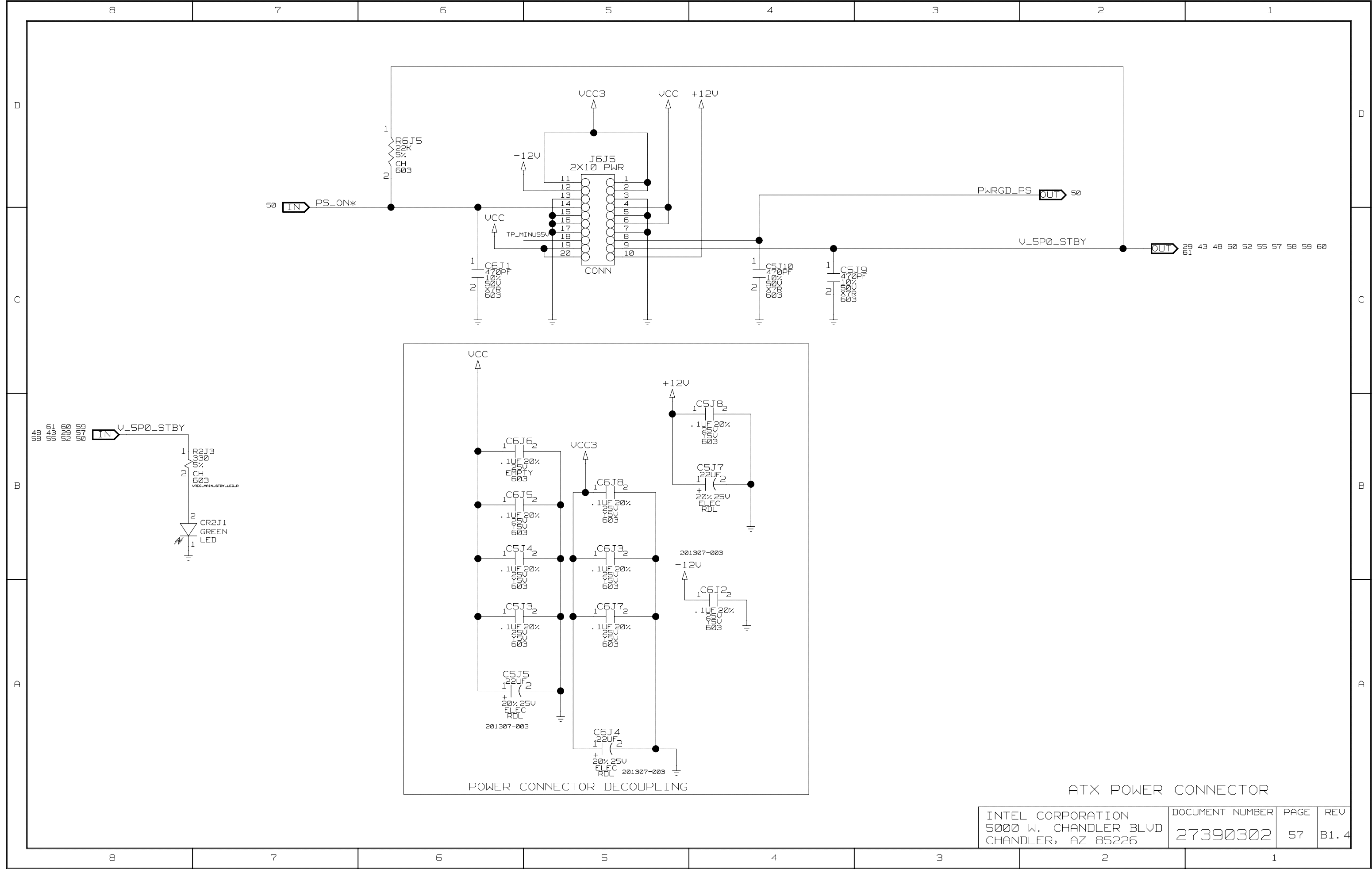
STUFFING OPTIONS DEPENDING ON CONTROLLER

LOCATION	NCP1570	TPPM0115
C5J1	STUFF 0.01UF	EMPTY
C5H5	STUFF 0.1UF	EMPTY
R5H3	EMPTY	STUFF 0-OHM

2P5 VREG

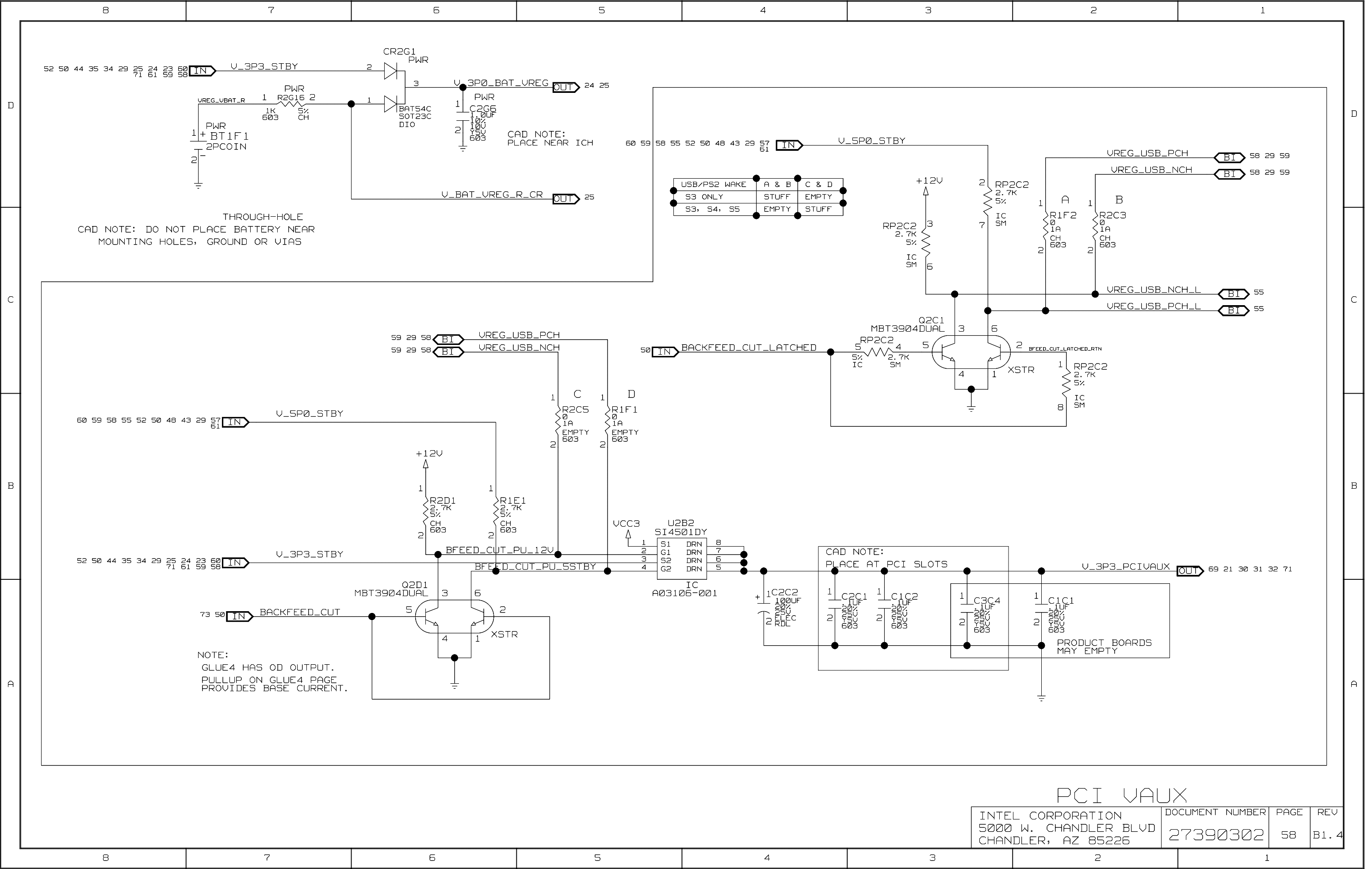
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ATX POWER CONNECTOR

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THROUGH-HOLE
CAD NOTE: DO NOT PLACE BATTERY NEAR
MOUNTING HOLES, GROUND OR VIAS

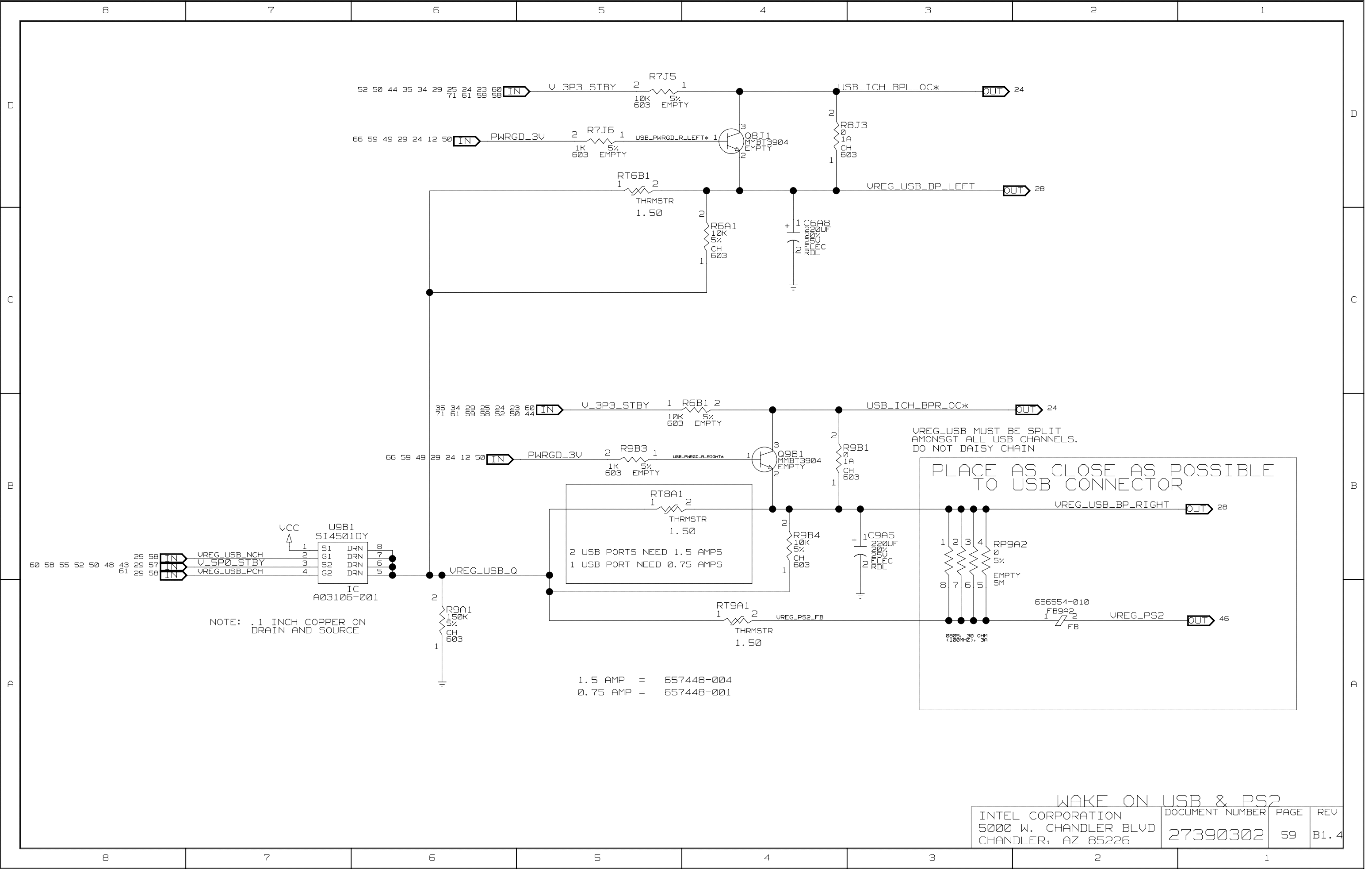
USB/PS2 WAKE	A & B	C & D
S3 ONLY	STUFF	EMPTY
S3, S4, S5	EMPTY	STUFF

NOTE:
GLUE4 HAS OD OUTPUT.
PULLUP ON GLUE4 PAGE
PROVIDES BASE CURRENT.

CAD NOTE:
PLACE AT PCI SLOTS

PCI VAUX

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NOTE: .1 INCH COPPER ON DRAIN AND SOURCE

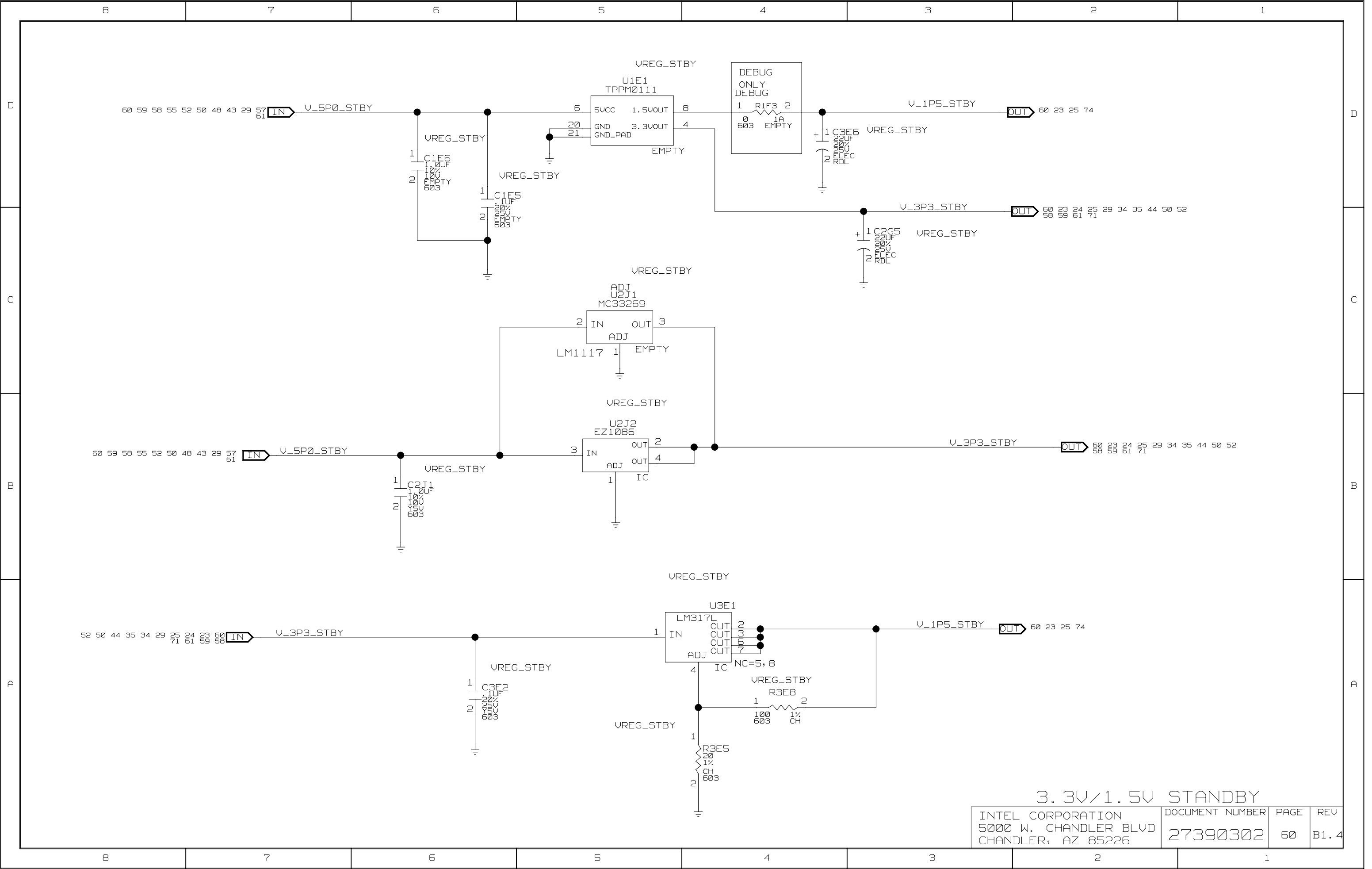
1.5 AMP = 657448-004
0.75 AMP = 657448-001

VREG_USB MUST BE SPLIT AMONGST ALL USB CHANNELS. DO NOT DAISY CHAIN

PLACE AS CLOSE AS POSSIBLE TO USB CONNECTOR

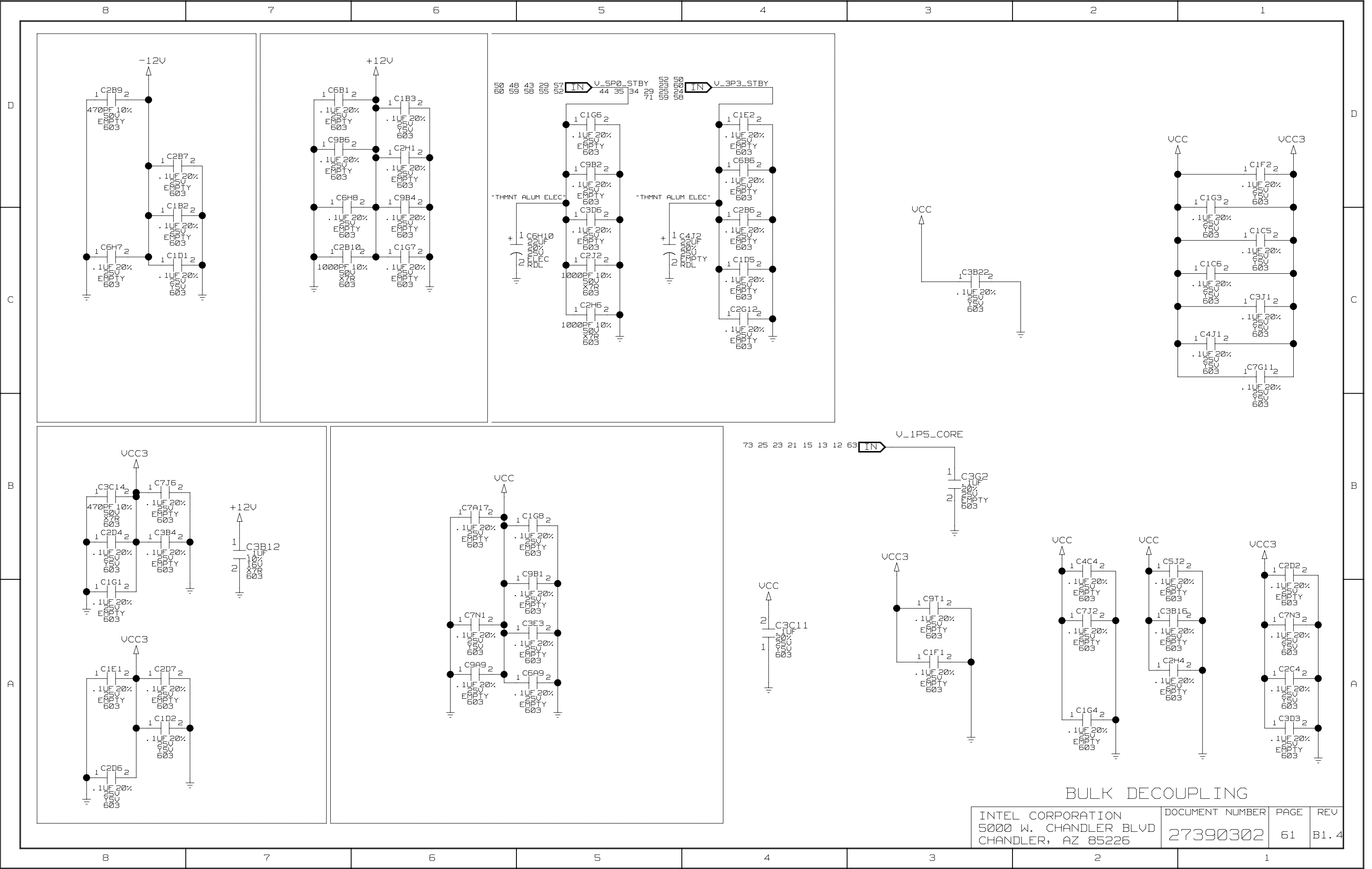
WAKE ON USB & PS2

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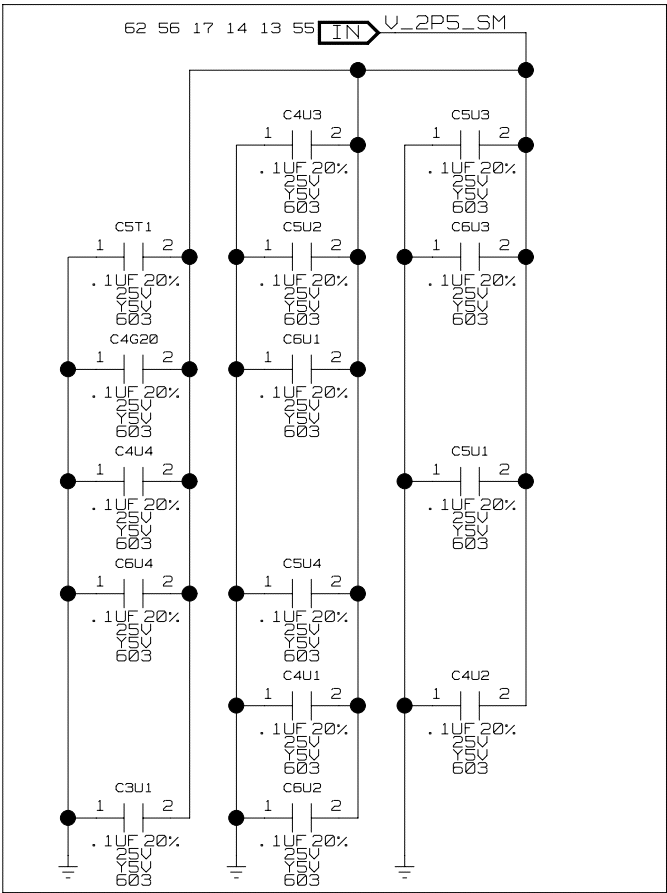


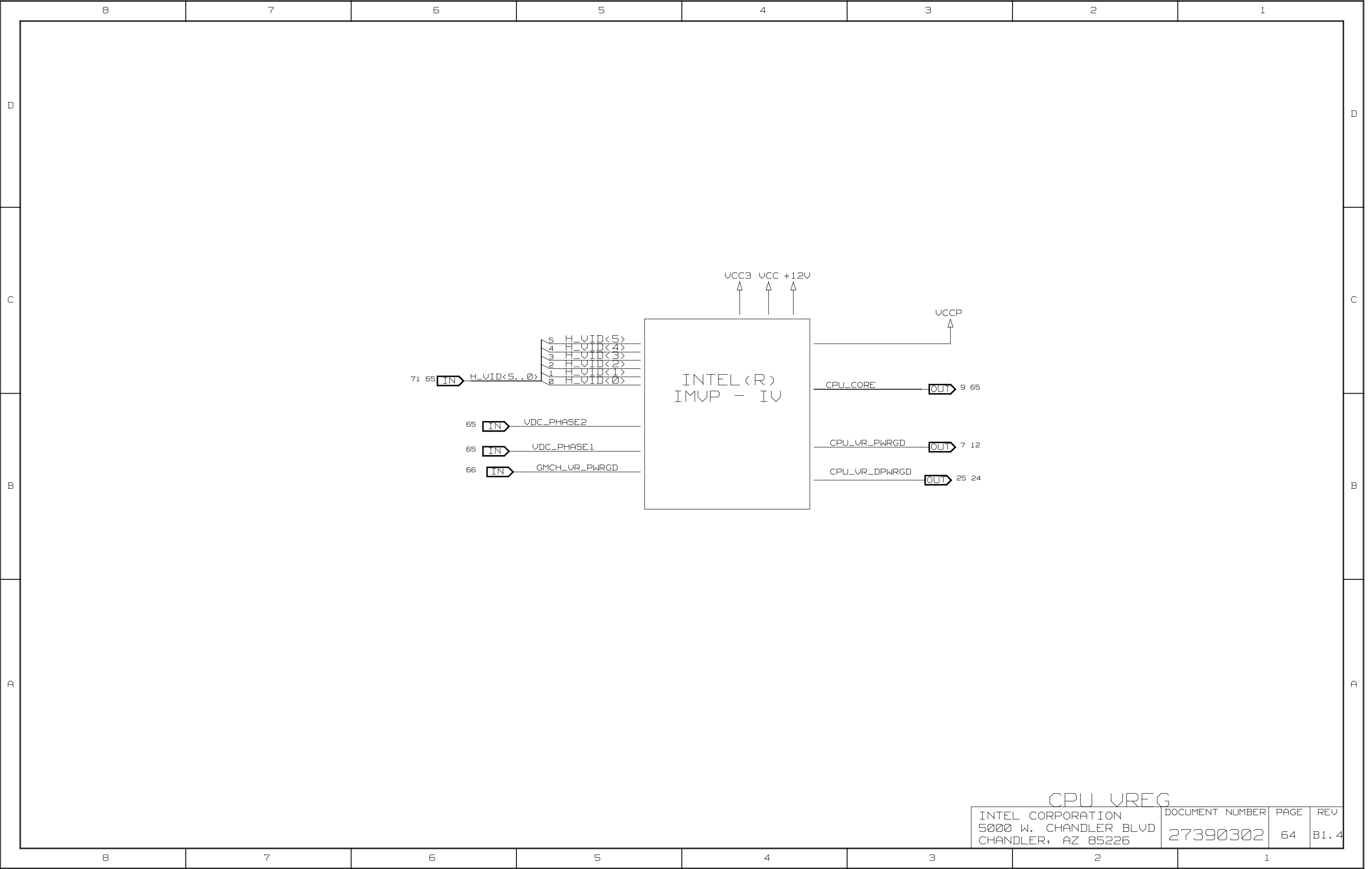
3.3V/1.5V STANDBY

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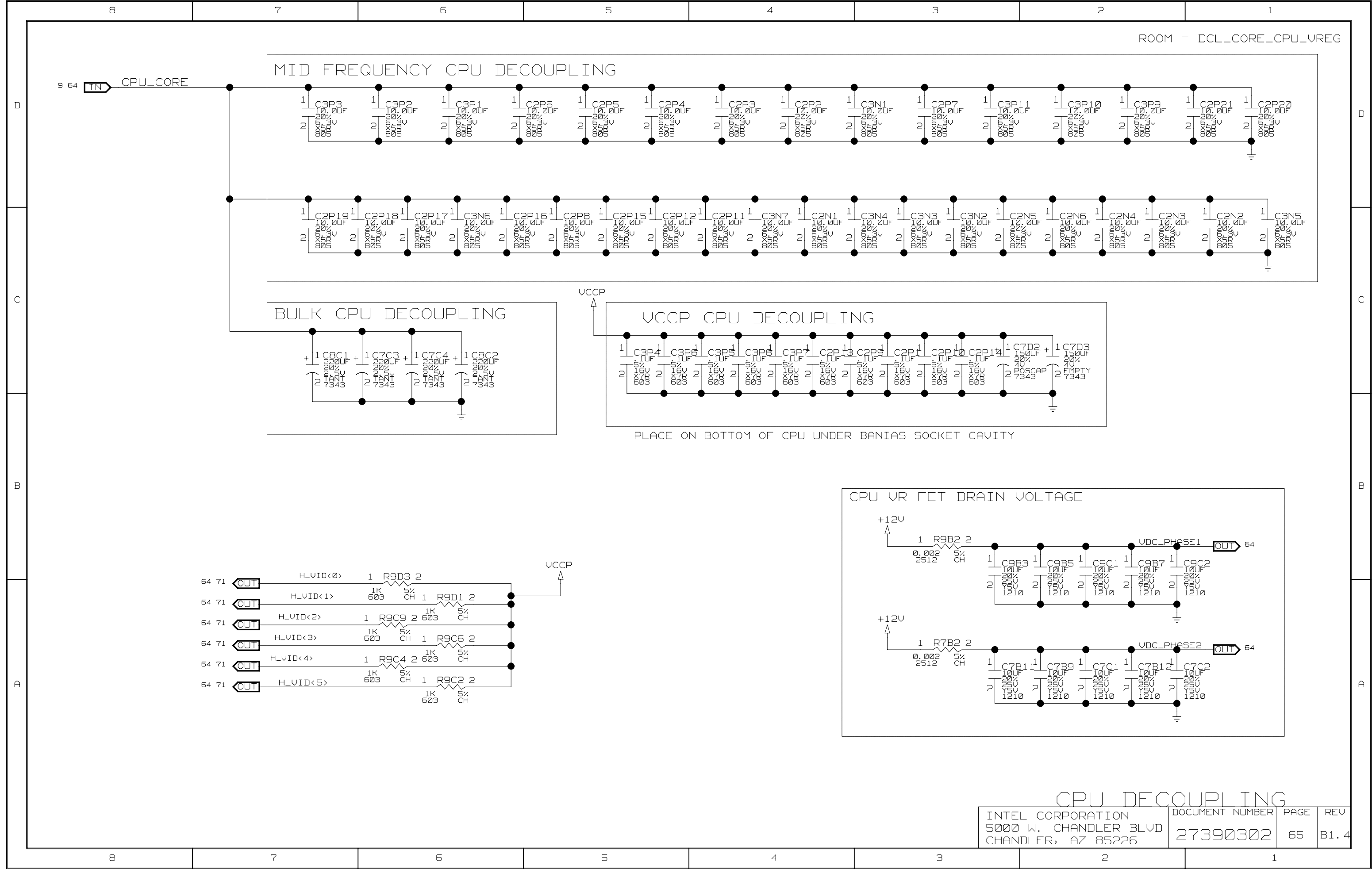
BULK DECOUPLING

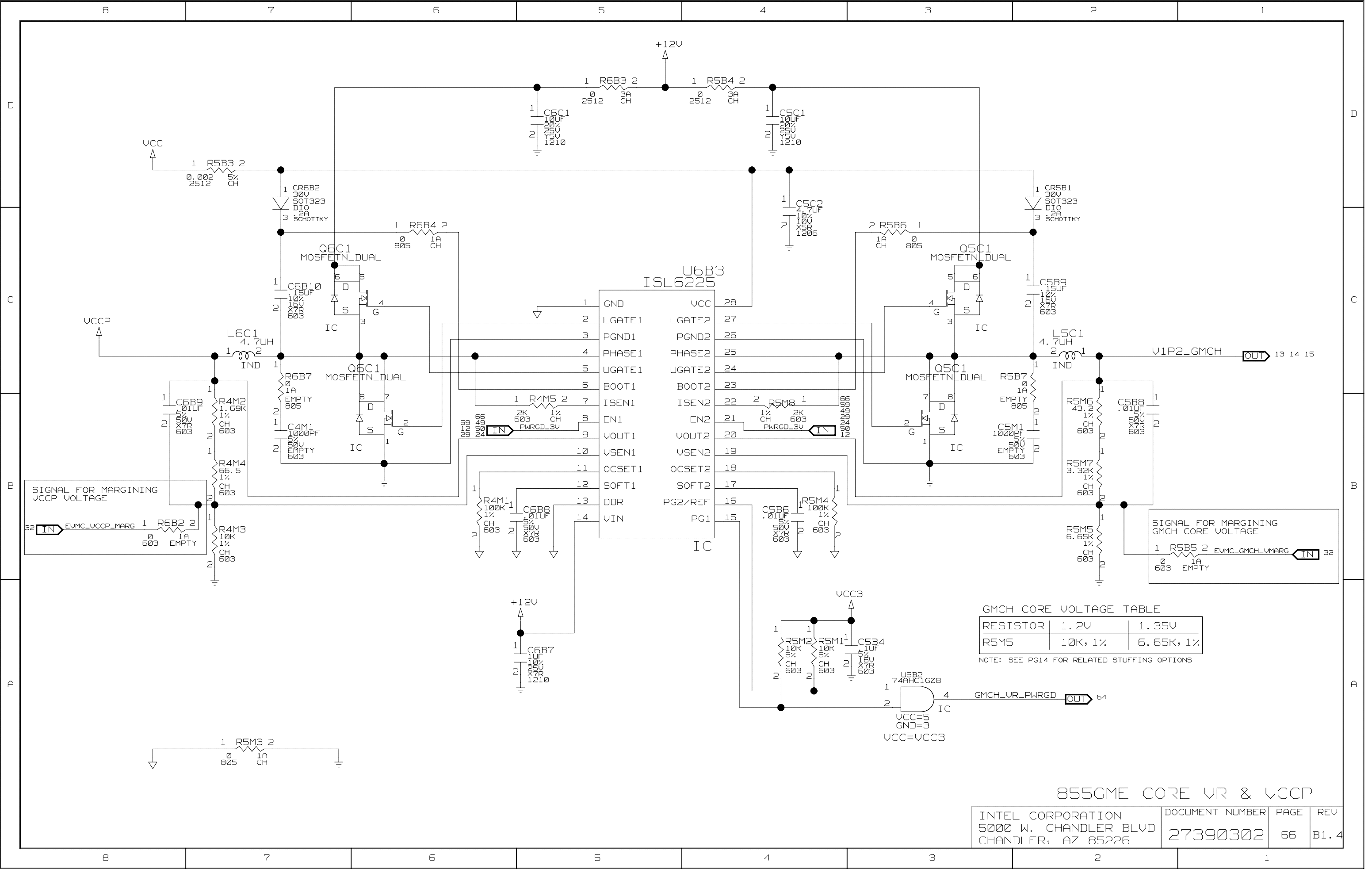




CPU VREG

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GMCH CORE VOLTAGE TABLE

RESISTOR	1.2V	1.35V
R5M5	10K, 1%	6.65K, 1%

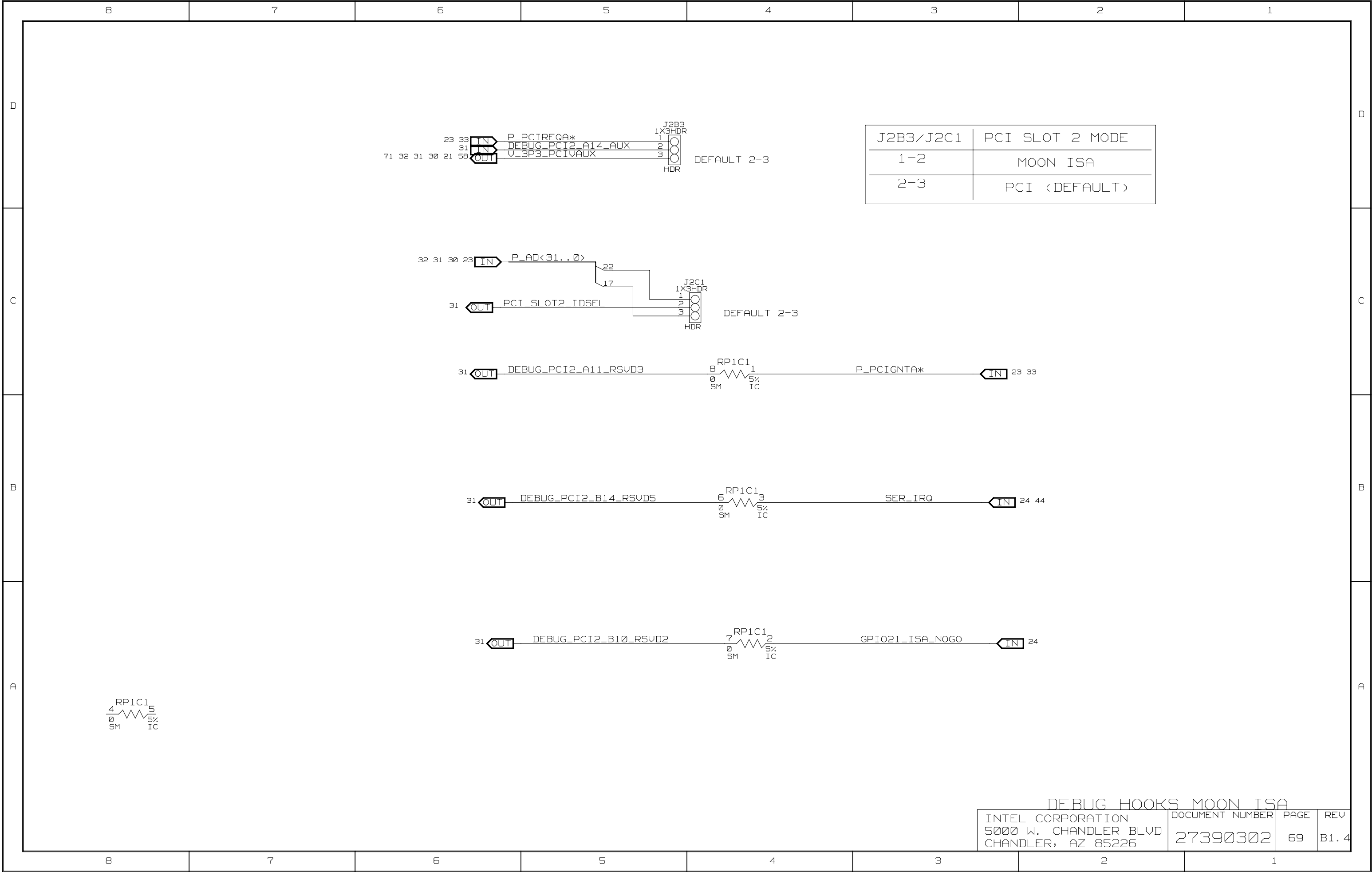
NOTE: SEE PG14 FOR RELATED STUFFING OPTIONS

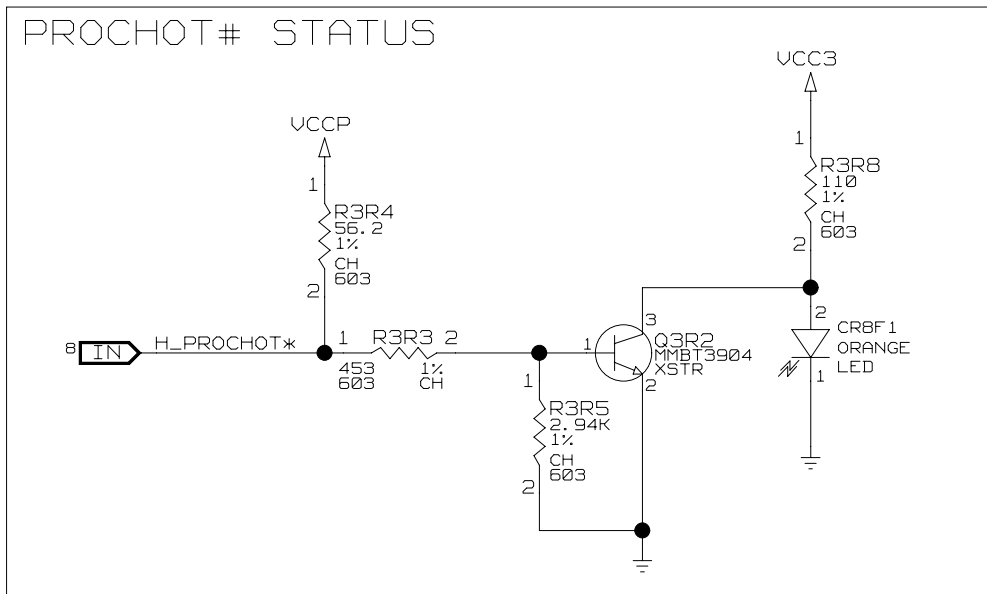
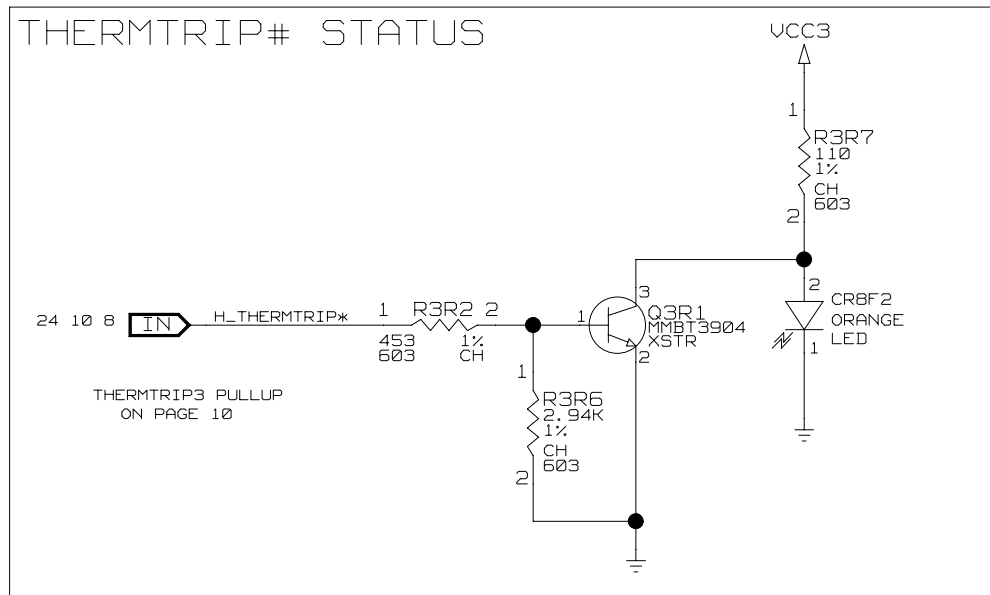
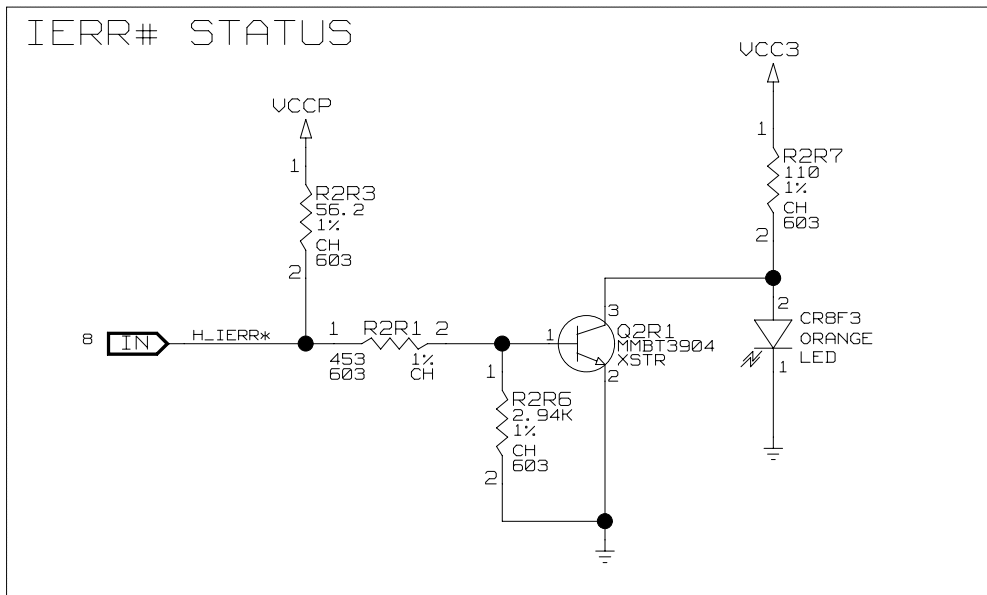
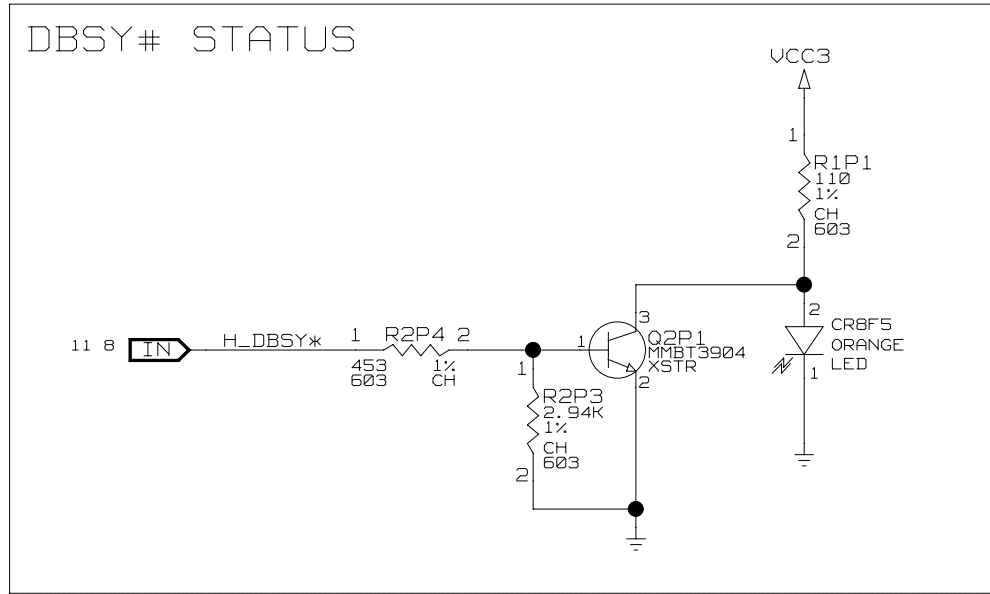
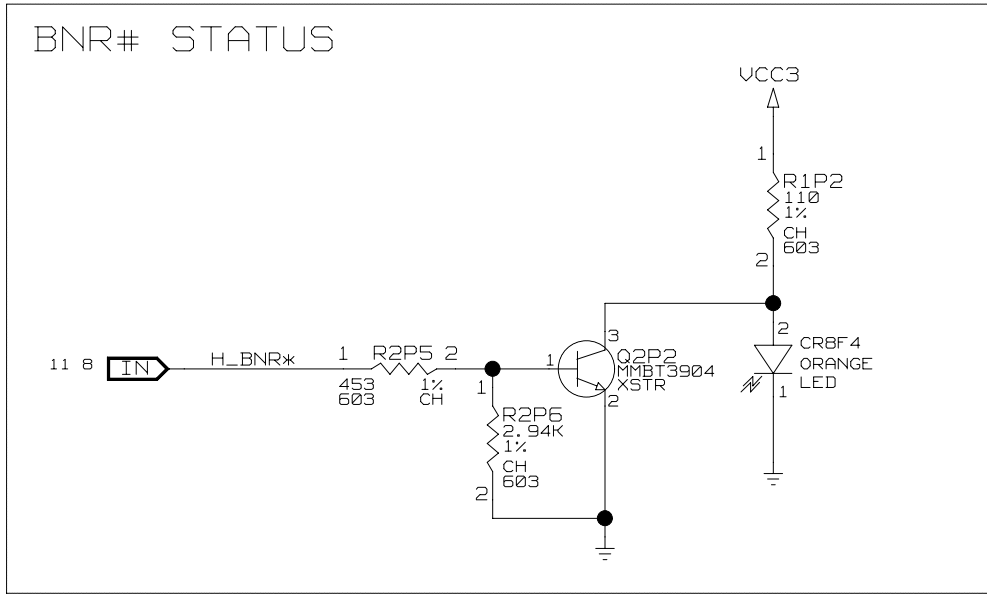
855GME CORE VR & VCCP

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8		7		6		5		4		3		2		1	

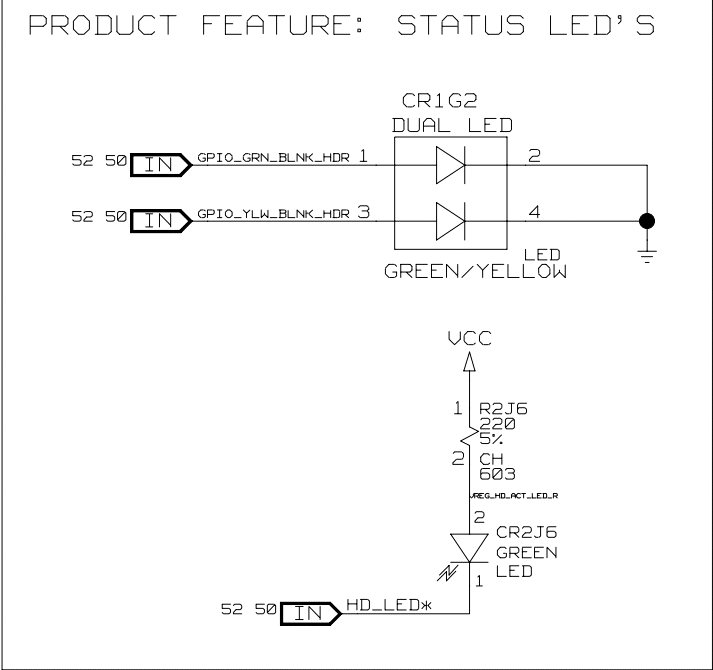
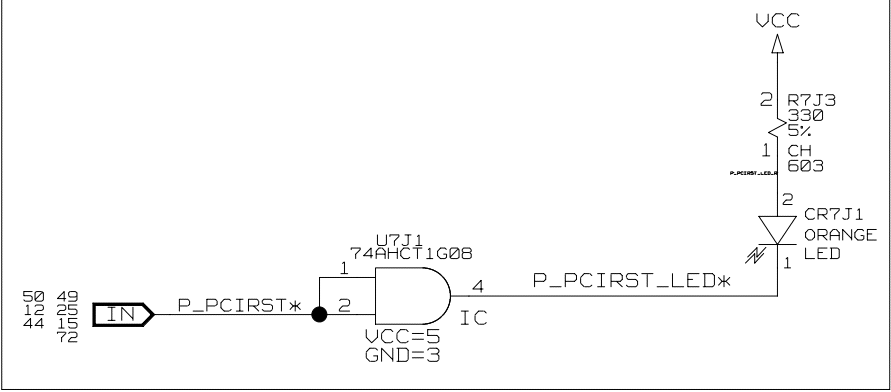
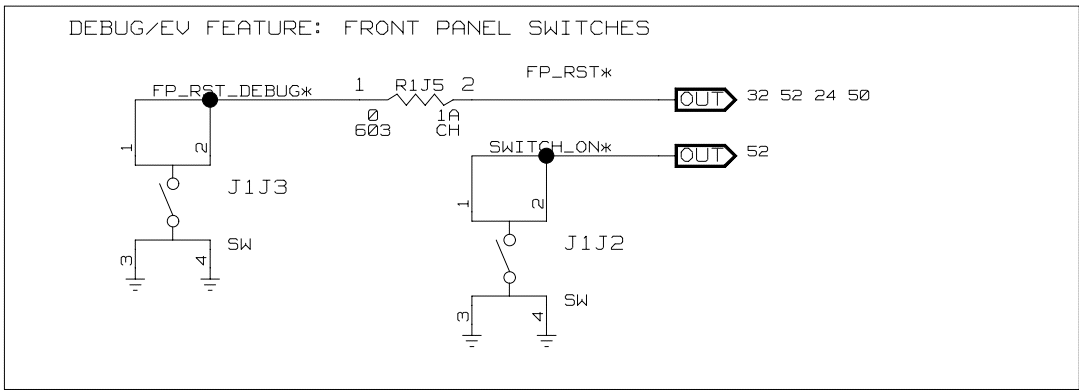
DEBUG PAGES





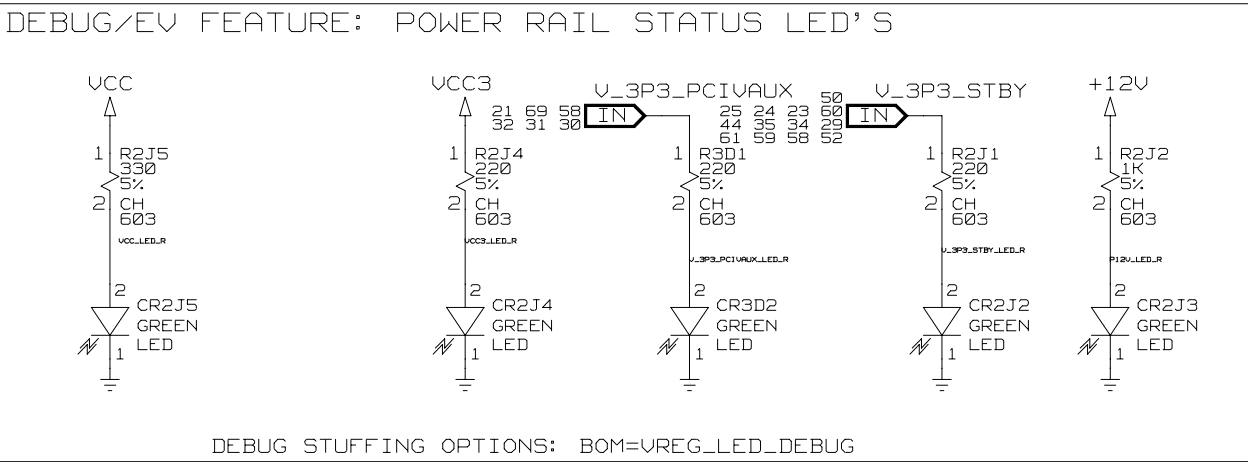
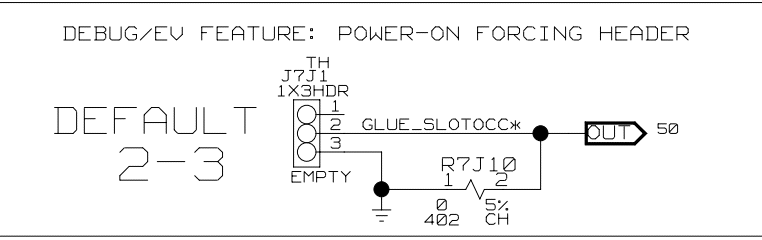
CPU STATUS LEDS

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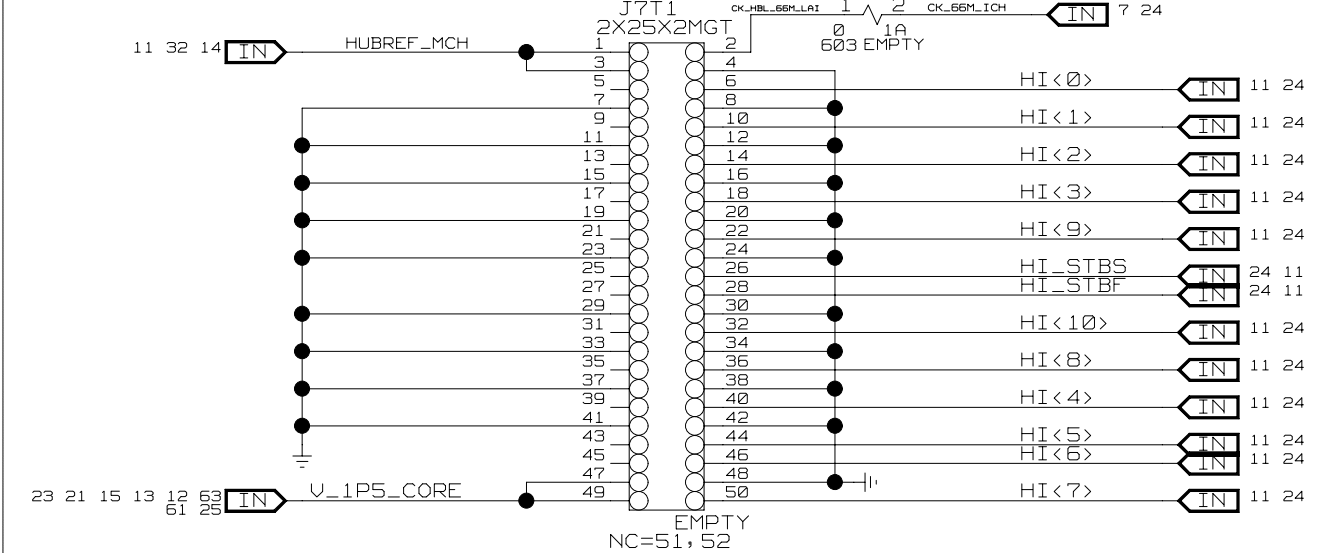
DEBUG/EV FEATURE: VID JUMPERS

VID	5	4	3	2	1	0	VCORE
0	0	0	0	0	0	0	1.708
0	0	0	0	0	1	0	1.692
0	0	0	0	1	0	0	1.676
0	0	0	0	1	1	0	1.660
0	0	0	1	0	0	0	1.644
0	0	0	1	0	1	0	1.628
0	0	0	1	1	0	0	1.612
0	0	0	1	1	1	0	1.596
0	0	1	0	0	0	0	1.580
0	0	1	0	0	1	0	1.564
0	0	1	0	1	0	0	1.548
0	0	1	0	1	1	0	1.532
0	0	1	1	0	0	0	1.516
0	0	1	1	0	1	0	1.500
0	0	1	1	1	0	0	1.484
0	0	1	1	1	1	0	1.468
0	1	0	0	0	0	0	1.452
0	1	0	0	0	1	0	1.436
0	1	0	0	1	0	0	1.420
0	1	0	0	1	1	0	1.404
0	1	0	1	0	0	0	1.388
0	1	0	1	0	1	0	1.372
0	1	0	1	1	0	0	1.356
0	1	0	1	1	1	0	1.340
0	1	1	0	0	0	0	1.324
0	1	1	0	0	1	0	1.308
0	1	1	0	1	0	0	1.292
0	1	1	0	1	1	0	1.276
0	1	1	1	0	0	0	1.260
0	1	1	1	0	1	0	1.244
0	1	1	1	1	0	0	1.228
0	1	1	1	1	1	0	1.212



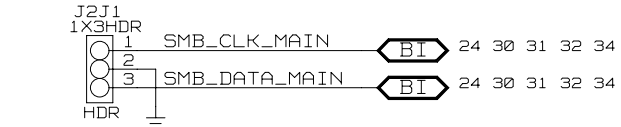
DEBUG/EV FEATURE: HUBLINK LAI HEADER

NOTE: BACKSIDE PART 700000-450 PLACE AT MIDPOINT OF HUBLINK ROUTING

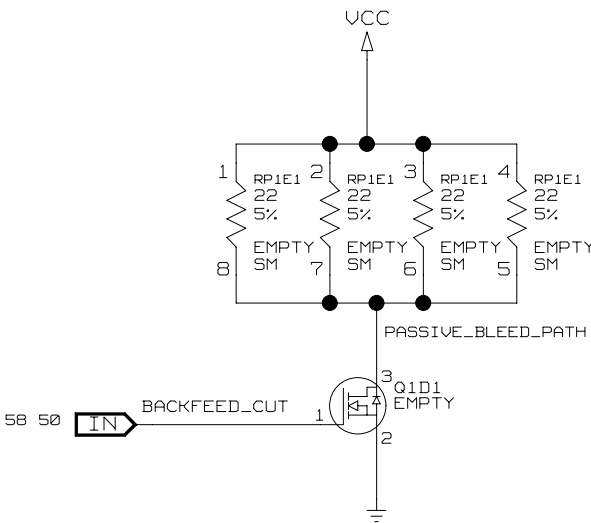


SOLDER MASK PADS: 5, 9, 13, 17, 21, 25, 27, 31, 35, 39, 43, 45
PINS ARE NOT ASSIGNED TP SIGNAL NAMES (PREVENTS TRACE CONNECTION)

DEBUG/EV FEATURE: SMBUS LAI HEADER



CUSTOMER C
PASSIVE BLEED CIRCUIT

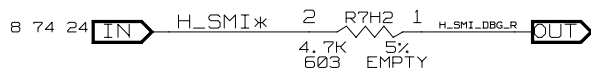


CAD NOTE: PLACE ON BACKSIDE, KEEP DP TRACE SHORT

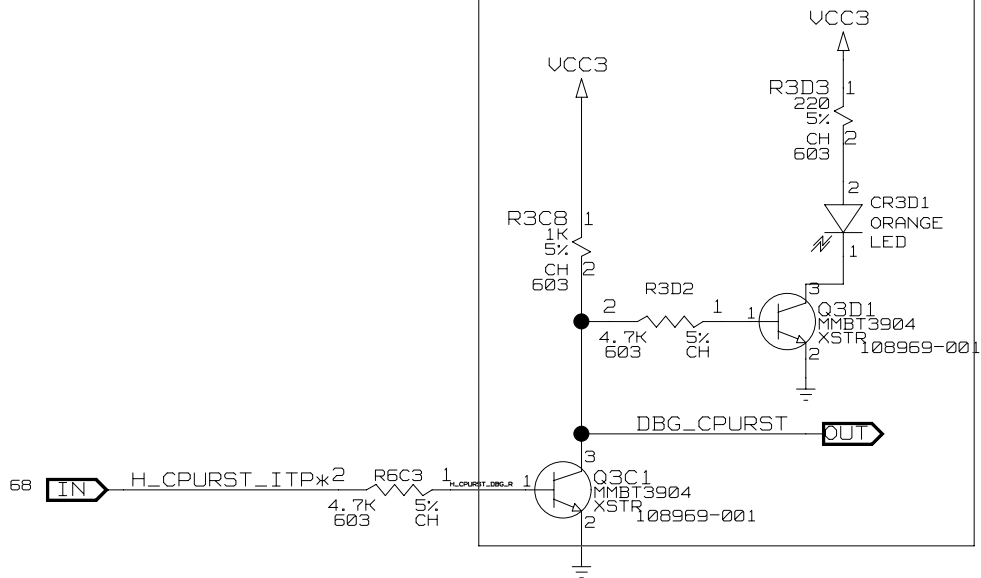
DEBUG/EV FEATURE: TDR COUPONS



DEBUG/EV FEATURE: INVERTING LEVEL SHIFTERS
ON FSB SIGNALS FOR DIAG LED'S



CAD NOTE:
PLACE UNDER DIMMS



CAD NOTE:
PLACE BY CPU

HUBLINK PROBE, TDR COUPONS, L.F.D.S.

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REVISION HISTORY

FAB B - REV 1.3

REMOVED UNSUPPORTED SPEED

FAB B - REV 1.4

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*****
*****      ALL REFERENCE POINTS FOR CFCFS FROM 855GM TO 805GME *****
*****      DURING NON-FLIGHT OPERATIONS IN P2-LIGHT MODE NET IS ACTUALLY 1.35 AND 1.2, DEPENDING ON SPEED NEEDED *****
*****      US OCEANIC UPDATE STRAPPING TABLE *****
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REVISION HISTORY

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